DS_MKY44AD16A_V1.4E

STEP TECHNICA CO.,LTD.

CUnet Family

MKY44-AD16A

DATA SHEET

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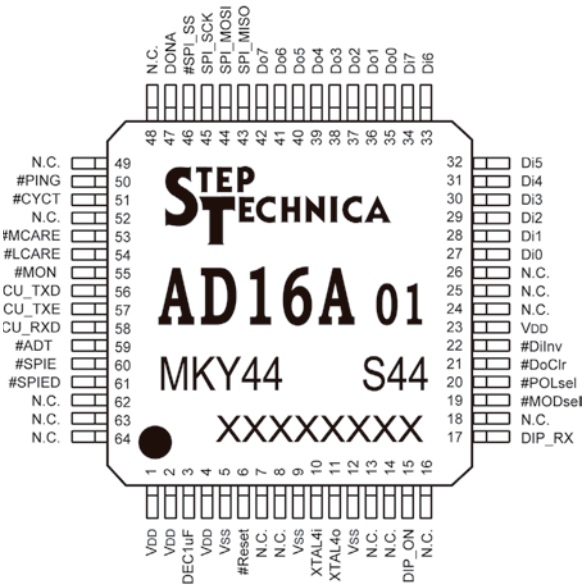
MKY44 Series CUnet-Compliant Intelligent Slave ICs

key words : 2ch 16 bits A/D 4 sampling methods 8 bits DI 8 bits DO

CUnet

■ MKY44-AD16A Specifications

- ● Model : MKY44-AD16A
- ● ADC : AD7682 external with SPI connection
- ● Number of channels : 2-channel multiplexer
- ● Loading mode
  - • Cyclic mode
  - • Single trigger mode (software trigger or hardware trigger)
  - • Moving average mode
  - • Period average mode
- ● Parameter settings for moving average mode and period average mode
  - • Sampling frequency (2 times, 4 times, 8 times, or 16 times)
  - • Sampling cycle (200 μs to 1 s, in units of 100 μ)
- ● DIO : 8 bits DI/8 bits DO
- ● Power voltage : 3.3 V
- ● Power consumption : 20 mA
- ● Temperature range : -40 to +85 °C
- ● Package : 64-pin TQFP (0.5 mm pitch 10 mm × 10 mm)
- ● ST44SW : Required



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

Specifications of Analog Devices A/D Converter AD7682

- ● Input
  - • Unipolar single end
  - • Differential (GND sense)
  - • Pseudo-bipolar
- ● Analog input range : 0 V to VREF (up to VDD)
- ● A/D conversion resolution : 16 bits
- ● Integral non-linearity error : Max. ±1.5 LSB/Normal ±0.5 LSB
- ● Number of channels : 4-channel multiplexer

■ Applications

Industrial devices
Medical devices
Measurement devices
Power wire monitoring
Process control

■ Overview

The MKY44-AD16A is a CUnet station IC with analog input function. With an MKY44-AD16A, analog and DIO control can be achieved on one chip without using the CPU, by connecting an AD7682 (Analog Devices AD converter) by SPI. The AD acquisition speed depends on the MKY44-AD16A. For analog input, the data acquisition timing can be selected from 4 modes. There are also parameter settings for smoothing processing. Measurement data according to the set mode is automatically input to the MKY44-AD16A's own memory block. The input data is automatically copied to all CUnet ICs through CUnet communication (memory sharing), so the user CPU can acquire analog data easily just by reading the memory blocks corresponding to each slave IC. Existing users of CUnet can get analog control just by adding this product to their networks. New users have the opportunity to reduce A/D control wiring that used to use parallel connections and to achieve easy, networked analog control.

■ Four Sampling Methods

A/D conversion in the MKY44-AD16A includes A/D conversion of the analog input of ch0, followed by A/D conversion of the analog input of ch1. The difference of sampling time for ch0 and ch1 is approximately 15 µs. The selected sampling method is shared by both ch0 and ch1. For period average and moving average, you can set the sampling interval and sampling frequency. You can also specify peak cut of the maximum value and the minimum value.

- Cyclic mode: CUnet executes communication regularly (cyclically). When "cyclic mode" is selected as the sampling method, the chip will execute A/D conversion for each cycle of CUnet and store the latest analog value in its occupied area (henceforth "self-owned area") within the shared memory of CUnet. The cycle time of CUnet communication is a constant value depending on transfer rate and other factors. For example, the cycle time is 155 µs in a system with 4 nodes at 12 Mbps.

- Single trigger mode: In single trigger mode, there are "hardware trigger mode" and "software trigger mode." If hardware trigger mode is selected, the MKY44-AD16A will execute A/D conversion when a bit selected from bits Di0 to Di7, which correspond to the eight general-purpose input pins, transits from "1" to "0," and it will store the analog value in the shared memory. If software trigger mode is selected, the master MKY43 can set the trigger data and address for the MKY44-AD16A. The chip will execute A/D conversion and store the analog value in its self-owned area when the data of that address transits to the specified data.

- Period average mode: For the sampling interval, you can set 200 µs to 1 s. For the sampling cycle, you can set 2, 4, 8, or 16 (4, 6, 10, or 18 when in peak cut). The MKY44-AD16A stores in the self-owned area the average value of A/D conversion data corresponding to the predetermined sampling interval and sampling frequency. The factory default sampling interval is 1 ms (1 kHz). The factory default sampling frequency is 8 times. With these settings, the interval at which the period average data is updated in the self-owned area is 8 ms "without peak cut" of the maximum and minimum values and 10 ms "with peak cut."

- Moving average mode: The MKY44-AD16A stores in the self-owned area the moving average value of the A/D conversion data corresponding to the predetermined sampling interval and sampling frequency. The sampling interval and frequency are the same as in period average mode. With the factory default settings (sampling interval 1 ms, sampling frequency 8 times), the interval at which the moving average data is updated in the shared memory is 1 ms, the same as the sampling interval.

Note: If period average or moving average mode is selected, the MKY44-AD16A will not participate in the network until the first average data is generated after returning from a reset. In such a case, the chip might take as long as 18 seconds before participating in the network depending on the settings for peak cut, sampling frequency, and sampling interval.

■ Data Placement of the Occupied Memory Block

The MKY44-AD16A occupies one MB (memory block) corresponding to the specified SA value. The MB occupied by the MKY44-AD16A is 8 bytes (64 bits). The data configuration within the 8 bytes is as follows.

Address	0x07	0x06	0x05	0x04	0x03	0x02	0x01	0x00
bit	63 to 56	55 to 48	47 to 40	39 to 32	31 to 16		15 to 0	
	SN	Status	EDo	Di7 to Di0	ch1 Analog Value		ch0 Analog Value	

55	54	53	52	51	50	49	48
Stype1	Stype0	MODsel	SPIE	TRGsel	DiInv	PCsel	POLsel

When other devices connected to CUnet need to refer to the input value of the analog input terminal with the MKY44-AD16A, they can simply read the memory block occupied by the MKY44-AD16A. Details follow.

(1) To refer to the analog value of ch0, read bits 15 to 0. To refer to the analog value of ch1, read bits 31 to16.
Since the data is in little endian format, lower bits represent lower address positions. Whether the analog values of ch0 and ch1 are Bipolar (0x8000 to 0x0000 to 0x7FFF) or Unipolar (0x0000 to 0xFFFF) is shown in the POLsel bit of bit 48. The POLsel bit of a Bipolar device is "1." The analog value shown right after the MKY44-AD16A returns from reset depends on the sampling method. If the sampling method is single trigger mode, "0x000" will be shown until the first single trigger is received after returning from reset. During this time, "0x0" will be shown as the sequential number (SN) in bits 63 to 56. If the sampling method is not single trigger mode, the first A/D data will be shown after returning from reset.

(2) To refer to the status of the Di pins, read the 1 byte of bits 39 to 32. The data of the general-purpose input pins (Di7 to Di0) depends on the setting of pin #DiInv. The setting status of pin #DiInv is shown in the DiInv bit, bit 50. If DiInv is "0," the 1 byte data of bits 39 to 32 will be shown by positive logic. In such a case, the status of the eight general-purpose input pins will be shown as "0" when in Low-level and as "1" when in High-level. If the DiInv bit is "1," the data will be shown by negative logic. Thus, the status of the general-purpose input pin will be shown as "1" when at Low-level and as "0" when at High-level.

(3) EDo (Echo back Data out), the byte from bit 47 to bit 40, is the echo back of the general-purpose output pin data (Do) shown in the MB specified by DOSA setting. By referring to this byte, you can confirm that the data is successfully output to the general-purpose output pin.

(4) The byte from bit 55 to bit 48 shows the setting condition and status of MKY44-AD16A.

Bits 55, 54: Shows the setting of the sample method read out from pins Stype1 and Stype0 in DIP-SW-DOSA when returning from a reset.

Bits 53, 50, 48: Shows by positive logic the individual settings read out from pins #MODsel, #DiInv, and #POLsel when returning from a reset.

Bit 51: TRGsel (trigger method selection) shows the value read out from the flash ROM when returning from a reset, or the value from the mail settings.

Bit 49: PCsel (peak cut selection) shows the value read out from the flash ROM when returning from a reset , or the value from the mail settings.

Bit 52: SPIE (SPI Error) sets "0" if the connection with A/D conversion element is normal when sampling the analog value, or "1" if the connection is abnormal.

(5) The 1 byte from bit 63 to 56 show a sequential number (SN) that is increased by "0x01" for each update of the A/D conversion data. By referring to this sequential number, you can see that the data has been updated even when the analog number of ch0 and ch1 remains the same as before.
The sequential number goes up in the order of "0x01, 0x02." After "0xFF," it goes back to "0x01." If the sampling method is single trigger mode, "0x00" will be shown right after returning from the reset.

Stype1 (bit 55)	Stype0 (bit 54)	Sampling method
"0"	"0"	Cyclic
"0"	"1"	Single trigger
"1"	"0"	Period average
"1"	"1"	Moving average

	Description	"1"	"0"
MODsel (bit 53)	MODE selection	Setting mode	Operation mode
SPIE (bit 52)	SPI error	Abnormal	Normal
TRGsel (bit 51)	Trigger method selection	Software trigger	Hardware trigger
DiInv (bit 50)	Di logical inversion selection	Logical inversion	No logical inversion
PCsel (bit 49)	Peak cut selection	Cut the maximum and minimum values	Do not cut the maximum and minimum values
POLsel (bit 48)	Analog type selection	Bipolar: ±n V input	Unipolar: 0 V to +n V input

■ Output to the General-Purpose Output Pins

The MKY44-AD16A outputs to the general-purpose output pin the 1 byte data of bits 39 to 32 within the MB corresponding to the DOSA value. The part labeled "d.c." (don't care) in the table does not influence the operation of the MKY44-AD16A.

Address	0x07	0x06	0x05	0x04	0x03	0x02	0x01	0x00
bit	63 to 40			39 to 32	31 to 0			
	d.c.			Do7 to Do0	d.c.			

39	38	37	36	35	34	33	32
Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0

■ DIP-SW Settings for SA/DOSA

MKY44-AD16A reads out the 16 bits of hardware setting data as serial data from the ST44SW, a dedicated LSI, when returning from hardware reset. It is recommended to connect two 8-bit type DIP-SWs to an ST44SW specified for hexadecimal.
The pins to connect a DIP-SW to the ST44SW are pulled up internally when reading from the DIP-SW. These bits recognize the ON state (Low-level) as "1". The following shows MKY44-AD16A's definitions for the bits of the DIP-SWs for setting.

Pin	Name	DIP-SW No.		Signal		Function/Description
1	#P17	DIP•SW•DOSA	8	Stype1		Select the sampling method for the analog value. Stype1, Stype0 = OFF, OFF Cyclic Stype1, Stype0 = OFF, ON Single trigger Stype1, Stype0 = ON, OFF Period average Stype1, Stype0 = ON, ON Moving average
32	#P16		7	Stype0		
31	#P15		6	DOSA	DOSA5	Set DOSA value in hexadecimal, treating the ON state as "1"
30	#P14		5		DOSA4	
29	#P13		4		DOSA3	
28	#P12		3		DOSA2	
27	#P11		2		DOSA1	
26	#P10		1		DOSA0	
21	#P07	DIP•SW•SA	8	BPS	BPS1	Set the transfer rate of CUnet. BPS1, BPS0 = OFF, OFF 12 Mbps BPS1, BPS0 = OFF, ON 6 Mbps BPS1, BPS0 = ON, OFF 3 Mbps BPS1, BPS0 = ON, ON (This setting is disabled.)
20	#P06		7		BPS0	
19	#P05		6	SA	SA5	Set SA value in hexadecimal, treating the ON state as "1"
18	#P04		5		SA4	
17	#P03		4		SA3	
16	#P02		3		SA2	
15	#P01		2		SA1	
14	#P00		1		SA0	

The ST44SW has a function that can set SA and DOSA in decimal. For details on setting in decimal, refer to the User's Manual of ST44SW.

■ Setting of Pins #MODsel, #POLsel, #DoClr, and #DiInv

The MKY44-AD16A has pins #MODsel, #POLsel, #DoClr, and #DiInv to set the functions. The MKY44-AD16A obtains the status of these setting pins when returning from a hardware reset. Activate the MKY44-AD16A after setting these pins to fit the user application.

MKY44-AD16A		Description	Function	
Pin	Name		Lo-input	Hi-input (open pin)
19	#MODsel	Mode selection	Setting mode	Operation mode
20	#POLsel	Analog type selection	Bipolar: ±n V input	Unipolar: 0 V to +n V input
21	#DoClr	Do pin clear selection when in DONA	Clear Do pin when in DONA	Do not clear Do pin when in DONA
22	#DiInv	Di logical inversion selection	Logical inversion	No logical inversion

When the MKY44-AD16A returns from hardware reset, the setting conditions read out from pins #MODsel, #POLsel, and #DiInv are shown in bits 53 to 48 of the occupied memory block by "1" for Low-level and "0" for High-level.

■ Extended Use of the CUnet Mail Function

The MKY44-AD16A supports “product inquiry” and “parameter setting change” requests from the master using the CUnet mail function.

● Product Inquiry Using the Mail Function

Upon receiving a message in product inquiry format using the “CUnet ?” character string, the MKY44-AD16A replies to the sender using the basic format of the MKY44-AD16A (see below). You can make a product inquiry from any node that is a CUnet IC in MEM mode.

◆ Product Inquiry Format

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Ascii	**C**	**U**	**n**	**e**	**t**	**[sp]**	**?**	**[¥r]**
Hex	0x43	0x55	0x6E	0x65	0x74	0x20	0x3F	0x0D

◆ Basic Format of the MKY44-AD16A

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Ascii	**A**	**D**	**1**	**6**	**A**	**[sp]**	***VN**	***Vn**
Hex	0x41	0x44	0x31	0x36	0x41	0x20	✻	✻

Address	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Ascii	**M**	✻	✻	✻	✻	✻	✻	✻
Hex	0x4D	0x00	SA	DOSA	ST1	ST2	0x00	0x00

Address	0x10	0x11	0x12	0x13	0x14	0x15	0x16	0x17
Hex	TP		FS	NS	TA		TD	TBM
	LSB	MSB			LSB	MSB		

◆ Description of the Basic Format

Symbol	Name	Description	Valid range
*VN *Vn	Version Number	Shows the version number of the MKY44-AD16A in two ASCII characters. The version numbers start from “01.” *VN represents the tens place and *Vn represents the ones place.	01 to 99 (in ASCII)
SA	DIP-SW-SA	Shows the DIP-SW-SA data shown in the section **“DIP-SW Settings for SA/ DOSA”** as one hexadecimal byte.	0x00 to 0xFF
DOSA	DIP-SW-DOSA	Shows the DIP-SW-DOSA data shown in the section **“DIP-SW Settings for SA/ DOSA”** as one hexadecimal byte.	0x00 to 0xFF
ST1	Status1	Shows the one-byte Status of bit 55 to 48 shown in **“Data placement of the occupied memory block”** (page 4 of this document).	0x00 to 0xFF
ST2	Status2	Bit 1 shows “1” when the output of pin #SPIED is Low. Bit 0 shows “1” when the setting of pin #DoClr is Low. Bits 2 to 7 are “0.”	0x00 to 0x03
TP	Time of Period	The setting value of the sample interval for the period average and moving average sampling methods is shown as two hexadecimal bytes (100 µs per unit). Only even numbers are valid.	0x0002 to 0x2710 (2 to 10000: even numbers) Initial value 0x000A
FS	Function Settings	Bit 1 is PCsel, bit 49, shown in **“Data placement of the occupied memory block.”** Bit 0 is TRGsel, bit 51, shown in **“Data placement of the occupied memory block.”**	0x00 to 0x03 Initial value 0x03
NS	Number of Sample	The setting value of the sampling frequency in the period average and moving average sampling methods is shown as one hexadecimal byte.	0x02/0x04/0x08/0x10 Initial value 0x08
TA	Trigger Address	If the sampling method is software trigger mode, the setting value of the trigger target address will be shown as two hexadecimal bytes. This address shows the address within the shared memory (Global Memory) of CUnet.	0x000 to 0x1FF Initial value 0x000
TD	Trigger Data	The setting value of the data of the trigger key, which functions when the sample method is single trigger by software trigger, is shown as one hexadecimal byte.	0x00 to 0xFF Initial value 0xFF
TBM	Trigger Bit Mask	The setting value of the bit mask to select the general-purpose input pin of the trigger target, which functions when the sample method is single trigger by hardware trigger, is shown as one hexadecimal byte. With this setting, only one bit (one pin) will be selected.	0x01/0x02/0x04/0x08 0x10/0x20/0x40/0x80 Initial value 0x01

● Parameter Setting Change Using the Mail Function

The MKY44-AD16A can change settings using the CUnet mail function. The settings that can be changed are TP (Time of Period), FS (Function Settings), NS (Number of Sample), TA (Trigger Address), TD (Trigger Data), and TBM (Trigger Bit Mask) in the basic format.

The mail format used in changing settings is different from the basic format of the MKY44-AD16A by one letter. The difference is "W" in byte 0x08 instead of "M." Therefore, it is recommended to change the settings by the following operation procedure.

Byte 0x08		Definition
Ascii	Hex	
M	0x4D	Master Code
W	0x57	Write
A	0x41	ACK (ACKnowledgement)
N	0x4E	NAK (Negative AcKnowledgement)
R	0x52	Read

1. First, execute "product inquiry" and copy the content sent from the MKY44-AD16A to the mail send buffer. Then, change "M" to "W" in byte 0x08.

2. Among TP, FS, NS, TA, TD, and TBM in the mail send buffer, rewrite the items to change.

3. Send a message to the MKY44-AD16A.

4-1. When the parameter settings are successfully changed using the mail function, the MKY44-AD16A sends a message in ACK format in which byte 0x08 of the basic format is "A." The changed values are stored in TP, FS, NS, TA, TD, and TBM in the ACK format.
When the MKY44-AD16A changes the parameter setting successfully using the mail function, the value is stored in the flash ROM installed in the MKY44-AD16A. Thus, even if the power of a MKY44-AD16A in normal mode is turned off and on, or if hardware reset is executed, the MKY44-AD16A will start operation using the changed values.

4-2. If the MKY44-AD16A could not change the setting successfully using the mail function, it will return a NAK code message in which byte 0x08 of the basic format is "N." In this case, the reason for the NAK will be shown in byte 0x09.

Setting change of MKY44-AD16A using the mail function is accepted only when in the setting mode where pin #MODsel is Low-level and when the message is sent from the node set to DOSA. If the setting change message is received when in normal mode where pin #MODsel is High-level, or if the message is sent from a node which is not set to DOSA, it will return the NAK code message and the setting will not be changed. Also, if the message does not match with the format or the value to change is not in the valid range, the MKY44-AD16A will return NAK code message and will not change the setting.

Byte 0x09	Definition
0x01	Cannot accept the setting change since it is not setting mode.
0x02	Cannot accept Write command from a node which does not match DOSA.
0x03	The received byte 0x09 (MC: Message Code) is not "0x00."
0x04	The specified TP (Time of Period) is out of the valid range.
0x05	The specified NS (Number of Sample) is out of the valid range.
0x06	The specified TA (Trigger Address) is out of the valid range.
0x07	The specified TBM (Trigger Bit Mask) is out of the valid range.
0x08	The specified FS (Function Settings) is out of the valid range.
0xE0	The first 8 bytes are irregular.
0xE1	The format is irregular.
0xE2	The mail data size is irregular.

If a message in which byte 0x08 of the basic format is "R" is sent to the MKY44-AD16A, you can receive ACK format where byte 0x08 is "A." This will enable reconfirmation of the changed settings.

To close the setting change using the mail function to start operation, execute hardware reset of the MKY44-AD16A by resetting the power in the normal mode where the High-level is set to pin #MODsel.

■ Configuration Example of the CUnet Analog Input Terminal with the MKY44-AD16A

As shown in the configuration diagram of the CUnet analog input terminal with the MKY44-AD16A, the signal of the MKY44-AD16A network interface (pins CU_TXE, CU_TXD, CU_RXD) is connected to CUnet via the recommended transceiver or pulse transformer. SPI is used to connect the MKY44-AD16A and Analog Devices, Inc.'s AD7682 (16 bit-ADC). If an input buffer or amplifier circuit is required in order to input the analog signal to AD7682, prepare a circuit that fits the application. If the voltage to input to AD7682 is ± nV (Bipolar), set the Low-level to pin #POLsel of the MKY44-AD16A. With this setting, A/D conversion data representing -32768 to 0 to 32767 (0x8000 to 0x0000 to 0x7FFF) will be stored in the shared memory of CUnet. If the voltage to input to AD7682 is 0V to +nV (Unipolar), set the High-level to pin #POLsel of the MKY44-AD16A. With this setting, A/D conversion data representing "0 to 65535(0x0000 to 0xFFFF)" will be stored in the shared memory of CUnet.

The MKY44-AD16A requires the ST44SW dedicated LSI to load DIP-SW settings. The MKY44-AD16A, upon hardware reset, starts operation, via the ST44SW, by reading its own station address (SA0 to 5), the transfer rate (BPS1, BPS0), the station address for controlling general-purpose output (DOSA0 to 5), and the sampling method for the analog signal (Stype1, Stype0).

If hardware trigger mode is selected as the sampling method, input to Di0 to Di7 a trigger signal whose Low-level and High-level are more than 100 μs.

If the data cannot be transmitted to the MKY44-AD16A, such as when the communication cable of the A/D slave configured with the MKY44-AD16A is disconnected or when the device to write the shared memory data in Do0 to Do7 goes out of communication, the DONA (DO Not Arrival) pin of the MKY44-AD16A will transit to High-level. Using the #DoClr pin setting, you can select whether to clear (set as "0x00") or maintain the general-purpose output pins Do0 to Do7 when the DONA pin transits from Low-level to High-level.

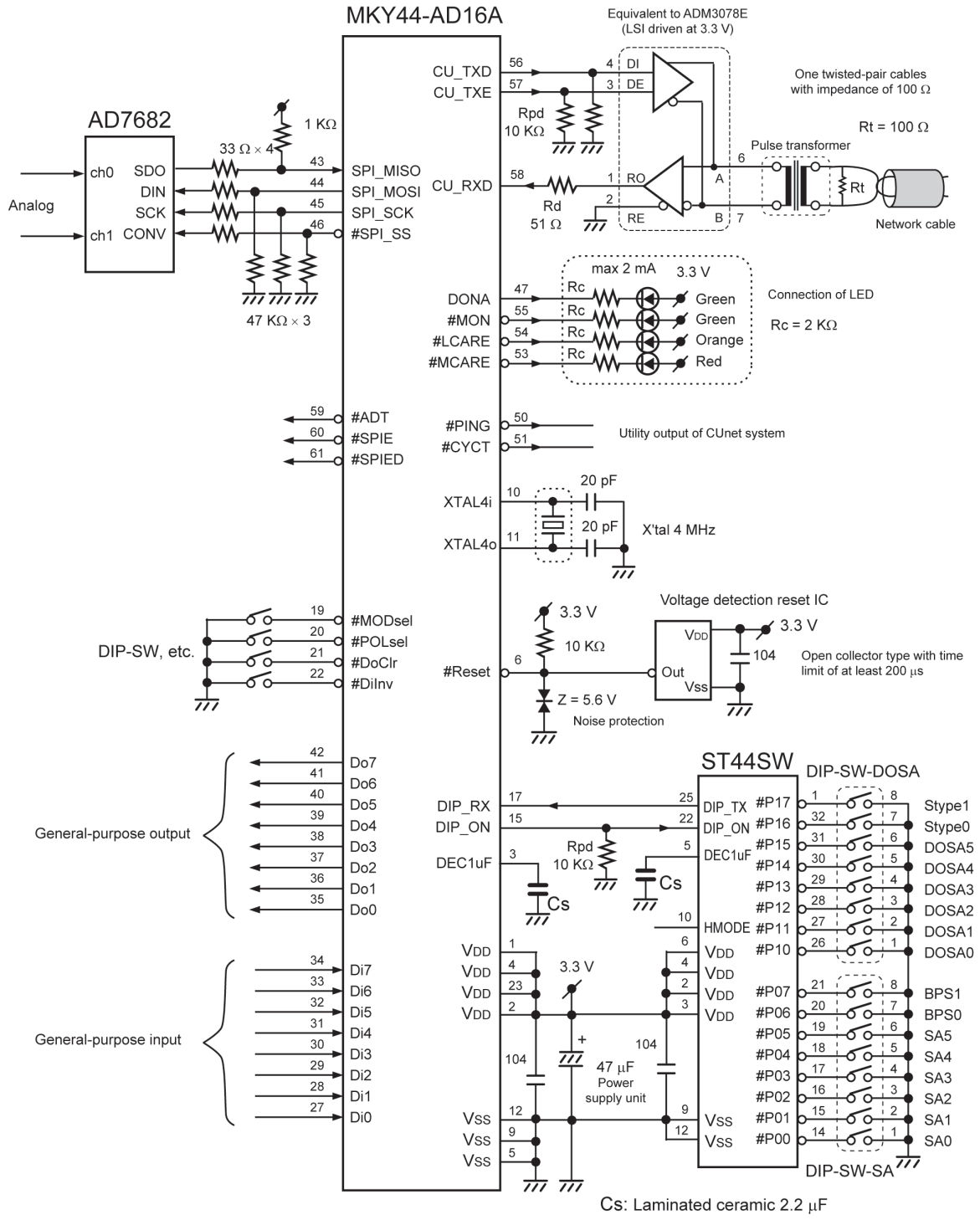
Even if the voltage of the analog input pin of AD7682 (16 bits-ADC) exceeds upper limit, or if it falls below lower limit, the value will not become cyclic (e.g. 0x0000 or 0x0001 before 0xFFFF) as the result of overflow. However, the value will not be guaranteed correct as an A/D conversion value. The voltage to apply to the analog input pins must be within the rated range.
Devices such as transceivers that drive CUnet communication cables will experience a large energy variation in signal transition. Similarly, if you need to control heavy load using general-purpose output pins, or if the drive performance of the signal source connected to general-purpose input pins is excessive, there will be a large energy variation in signal transition. To prevent the signal for A/D conversion from receiving adverse electrical effects from these, pay careful attention to the power supply ability of each power supplies, the arrangement of components on the board, and the wiring of signal cables. In particular, make sure that the signals involving CU_TXD, CU_TXE, and CU_RXD do not become parallel with or overlap the analog signals.

The MKY44-AD16A has an SPI connection monitor. When SPI connection is normal, the High-level is output to pin #SPIE (SPI Error). When it is abnormal, the Low-level is output to pin #SPIE. The output to this #SPIE pin is updated when the analog value is sampled. The MKY44-AD16A normally outputs the High-level to pin #SPIED (SPI Error Detect). However, after detecting an SPI connection error, it will continue outputting the Low-level to pin #SPIED until the next hardware reset. For applications in which SPI connection errors are detected, it is recommended to perform maintenance to enhance the quality and stability of the device peripheral environment and hardware.

■ Signal in A/D Conversion

The MKY44-AD16A outputs the Low-level to pin #ADT (A/D Timing) in A/D conversion. By monitoring this pin, you can confirm the execution of A/D conversion.

■ Configuration Diagram of the Analog Input Terminal



Cs: Laminated ceramic 2.2 μF

■ Pin Functions of the MKY44-AD16A

Pin name	Pin No.	Logic	I/O	Function
DEC1UF	3	--	--	Connect a capacitor whose effective capacitance is at least 1 µF and a 0.1 µF ceramic capafitor for high frequency bypass in parallel between this pin and Vss. Or connect a laminated ceramic capacitor of around 2.2 µF with the property that capacitance reduction is about 20% even in DC bias.
#Reset	6	Negative	I/O	The hardware reset input pin of MKY44-AD16A. Right after power is turned on or when the user intentionally resets the hardware, Low should be retained for at least 200 µs.
XTAL4i XTAL4o	10, 11	--	--	Pins to connect a crystal resonator. Connect a 4 MHz crystal resonator between these pins. Connect 20 pF ceramic capacitors between these pins and Vss. The layouts must be respectively near the pins. When connecting oscillator, input the clock signal to XTAL4i as shown below and leave XTAL4o to be opened. Clock frequency : 4 MHz ±500 ppm Jitter : Within 500 ps Rise / Fall time : Within 20 ns (VDD 20% - 80% threshold)
DIP_ON	15	Positive	O	Connect this pin with pin DIP_ON of the ST44SW. For more information about the ST44SW, refer to the ST44SW User's Manual.
DIP_RX	17	Positive	I	Connect this pin with pin DIP_TX of the ST44SW. For more information about the ST44SW, refer to the ST44SW User's Manual.
#MODsel	19	Negative	I	Pin to set the mode of the MKY44-AD16A.
#POLsel	20	Negative	I	Pin to set whether the analog input type should be treated as Bipolar (±n V) or Unipolar (0 V to+n V).
#DoClr	21	Negative	I	Setting pin to clear pins Do0 to Do7 when in DONA.
#DiInv	22	Negative	I	Pin to set logical inversion of Di0 to Di7.
Di0 to Di7	27 to 34	Positive	I	8 bits of general-purpose input pins. Leave these pins open when not in use (internal pull-up).
Do0 to Do7	35 to 42	Positive	O	8 bits of general-purpose output pins. Leave these pins open when not in use.
SPI_MISO	43	Positive	I	MISO function pin of SPI. Connect it to pin SDO of the AD7682.
SPI_MOSI	44	Positive	O	MOSI function pin of SPI. Connect it to pin DIN of the AD7682.
SPI_SCK	45	Positive	O	SCK function pin of SPI. Connect it to pin SCK of the AD7682.
#SPI_SS	46	Negative	O	#SS function pin of SPI. Connect it to pin CONV of the AD7682.
DONA	47	Positive	O	This pin retains the High-level during the DONA (DO Not Arrival) state. It is at Low-level at other times.
#PING	50	Negative	O	A pin to output the PING signal, which is a standard function of CUnet. When the PING signal occurs, this pin transitions to Low-level.
#CYCT	51	Negative	O	A pin to output the CYCT signal, which is a standard function of CUnet. When the CYCT signal occurs, this pin transitions to Low-level.
#MCARE	53	Negative	O	A pin to output the MCARE signal, which is a standard function of CUnet . This pin outputs the Low-level for about 50 ms, when the MCARE signal occurs and when it returns from hardware reset. It is recommended to connect red color LED indicating a definite warninf to this pin.
#LCARE	54	Negative	O	A pin to output the LCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for about 50 ms, when the LCARE signal occurs and when it returns from hardware reset. It is recommended to connect orange color LED indicating a gentle warning to this pin.
#MON	55	Negative	O	A pin to output the MON signal, which is a standard function of CUnet. This pin retains Low-level while a link has been established with another CUnet devices for at least 3 consecutive cycles. It is recommended to connect green color LED indicating a stable operation to this pin.
CU_TXD	56	Positive	O	Output pin to send CUnet packets. Connect this pin to a drive input pin such as of a driver.
CU_TXE	57	Positive	O	A pin to output the High-level while CUnet packets are output. Connect this pin to the enable input pin of the driver.
CU_RXD	58	Positive	I	A pin to input CUnet packets. Connect this pin to the output pin of the receiver.
#ADT	59	Negative	O	Monitor pin for A/D conversion operation. This pin outputs the Low-level during A/D conversion.
#SPIE	60	Negative	O	Pin monitoring the SPI connection state. This pin outputs the Low-level when an SPI error is active. The output of this pin is updated when the analog value is sampled.
#SPIED	61	Negative	O	This pin normally outputs the High-level, but outputs the Low-level from when an SPI connection error is detected until hardware reset.
Vdd	1, 2, 4, 23			Power pin. Supply 3.3 V.
Vss	5, 9, 12			Power pin. Connected to 0 V.
N.C.	7, 8, 13, 14, 16, 18, 24, 25, 26, 48, 49, 52, 62, 63, 64			Do not connect to other signals; keep them open.

■ Monitor pins of CUnet

Pin	Function
#PING	This pin normally maintains High-level. It transitions to Low-level when the PING instruction is received from another CUnet station, and later it transitions to High-level when a packet with no PING instruction to MKY44-AD16A is not placed is received from another CUnet station.
#CYCT	This pin normally maintains High-level and outputs Low pulse for "2 × Tbps" time at the lead timing of the CUnet cycle. Tbps is 83.33 ns at 12 Mbps, 166.67 ns at 6 Mbps, and 333.33 ns at 3 Mbps.
#MON	This pin outputs the MON signal, which is a standard function of CUnet. This pin retains Low-level while a link has been established with another CUnet station for at least 3 consecutive cycles.
#LCARE	This pin outputs the LCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for 50 ms when the LCARE signal is generated and upon return from hardware reset. Also, this pin outputs the Low-level to display hardware errors, including setting errors.
#MCARE	This pin outputs the MCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for 50 ms when the MCARE signal is generated and upon return from hardware reset. Also, this pin outputs the Low-level to display hardware errors, including setting errors.
DONA	This pin outputs the Low-level when the master set in DOSA is connected. When it has not confirmed the presence of another party in the past 16 consecutive cycles, it outputs the High-level.

■ Connection of LEDs and Display Status

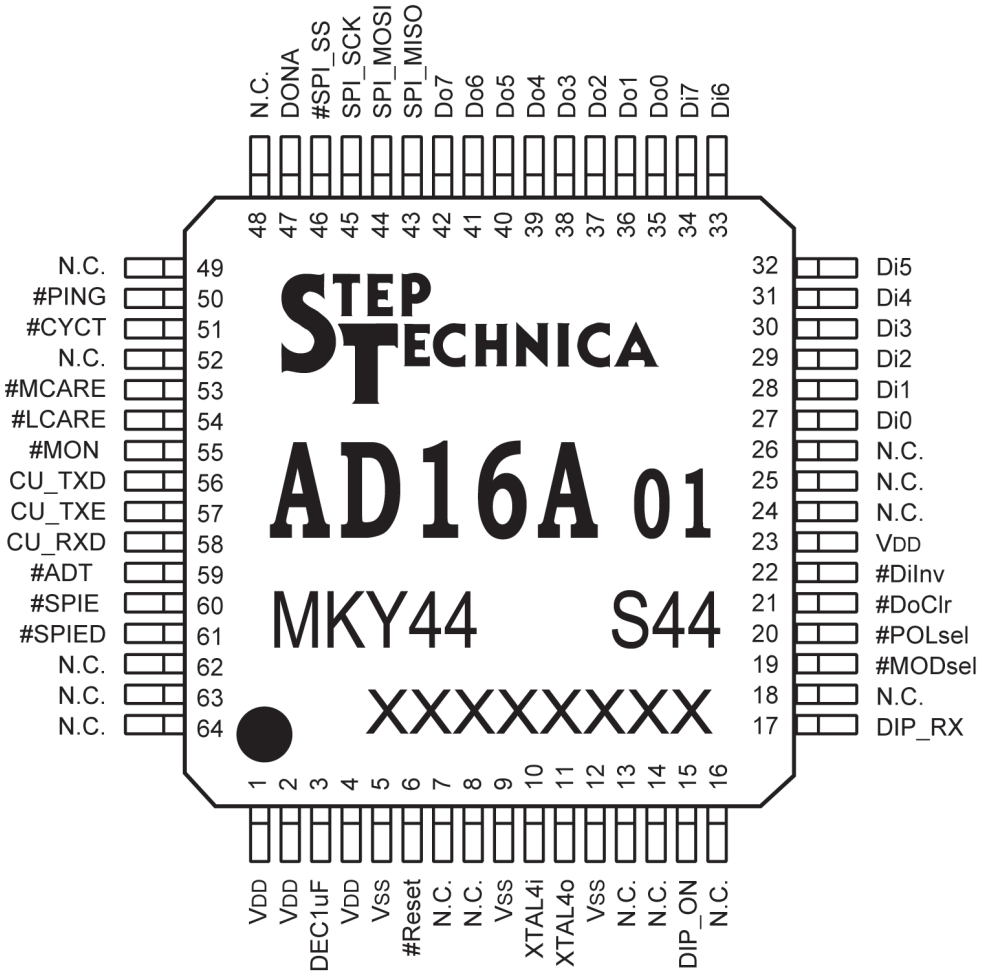
LED connection is recommended for the #MON, #LCARE, #MCARE, DONA pins of MKY44-AD16A. It is recommended to connect green color LED part indicating a stable operation to #MON pin and DONA pin. To #LCARE pin, it is recommended to connect orange color LED part indicating a gentle warning. To #MCARE pin, it is recommended to connect red color LED part indicating a definite warning. These pins have ±2mA current drive capability. Connect them in such a way that the LEDs will light up at Low-level.
The LEDs display the status of MKY44-AD16A. The state in which MON and DONA are lit is when normal operation is possible.
Note: The following table does not cover the pin name "#" that shows negative logic, since it is based on signal names.

DONA	MON	LCARE	MCARE	State
---	---	---	---	Indicates the state of power off, the state when the #Reset pin is active, or the state when no CUnet devices is linked after returning from hardware reset.
---	●	---	---	Although a link is successfully established with at least one CUnet device, the station address device (the other party that writes the data to the MKY44-AD16A) set by DOSA is missing.
●	●	---	---	The connection of the CUnet network is normal.
---	---	---	●	The setting values of SA and DOSA of DIP-SW are inappropriate.
---	---	□	---	When it becomes clear that at least one CUnet link is not established, the LED flashes for approximately 50 ms.
---	---	---	□	When it becomes clear that at least one CUnet link has not been established during the last 3 consecutive scans, the LED flashes for approximately 50 ms.
---	---	□	□	When it becomes clear that at least one CUnet link has been disconnected during the last 3 consecutive scans, and when hardware reset is executed, the LED flashes for approximately 50 ms.
---	---	▲	▲	The following internal hardware of MKY44-AD16A is abnormal. Blink alternately every second ⇒ DIP-SW read hardware including ST44SW Blink alternately every two seconds ⇒ MKY44-AD16A internal hardware Please perform maintenance such as replacement.

●: Continuous lighting □: Flash lighting for about 50 ms ▲: Alternating lit and unlit every few seconds

Unique to MKY44-AD16A display, the status in which only MCARE stays lit means that the settings of SA and DOSA of DIP-SW are inappropriately identical or overlapping values. If LCARE and MCARE keep blinking every few seconds, it means a failure caused by a crash in MKY44-AD16A.
The other signal transitions of MON, LCARE, and MCARE are standard CUnet operation. For more information about these signals, refer to the section ***"Quality Control and Indication of Network"*** and others in the User's Manual of the CUnet-dedicated LSI that is installed in the device to refer to the MKY44-AD16A data.

■ Pin Assignment



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

■ Electrical Ratings

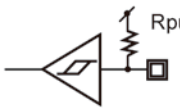
(T_A = 25°C V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	---	-55	---	125	°C
Operating temperature	Topr	---	-40	---	85	°C
Pin voltage (absolute maximum rating)	V_I	---	-0.3	---	V_{DD}+0.3	V
Operating power supply voltage	V_{DD}	---	3.0	3.3	3.6	V
Mean operating current	$V_{DD}A$	Vi = V_{DD} or V_{SS}, output open XTAL = 4 MHz	---	10	20	mA
I/O pin capacitance	Ci/o	V_{DD} = Vi = 0 V Ta = 25°C	---	10	---	pF
Rise/fall time of input signal	T_{ICLK}	When inputting generated clock of XTAL4i pin	---	---	5	ns
Rise/fall time of input signal	T_{IRF}	Schmitt trigger input	---	---	100	ms

■ Pin Ratings

No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type
1	--	V_{DD}	--	17	I	DIP_RX	A	33	I	Di6	A	49	--	N.C.	--
2	--	V_{DD}	--	18	--	N.C.	--	34	I	Di7	A	50	O	#PING	B
3	--	DEC1uF	--	19	I	#MODsel	A	35	O	Do0	B	51	O	#CYCT	B
4	--	V_{DD}	--	20	I	#POLsel	A	36	O	Do1	B	52	--	N.C.	--
5	--	V_{SS}	--	21	I	#DoClr	A	37	O	Do2	B	53	O	#MCARE	B
6	I/O	#Reset	C	22	I	#DiInv	A	38	O	Do3	B	54	O	#LCARE	B
7	--	N.C.	--	23	--	V_{DD}	--	39	O	Do4	B	55	O	#MON	B
8	--	N.C.	--	24	--	N.C.	--	40	O	Do5	B	56	O	CU_TXD	B
9	--	V_{SS}	--	25	--	N.C.	--	41	O	Do6	B	57	O	CU_TXE	B
10	--	XTAL4i	--	26	--	N.C.	--	42	O	Do7	B	58	I	CU_RXD	A
11	--	XTAL4o	--	27	I	Di0	A	43	I	SPI_MISO	A	59	O	#ADT	B
12	--	V_{SS}	--	28	I	Di1	A	44	O	SPI_MOSI	B	60	O	#SPIE	B
13	--	N.C.	--	29	I	Di2	A	45	O	SPI_SCK	B	61	O	#SPIED	B
14	--	N.C.	--	30	I	Di3	A	46	O	#SPI_SS	B	62	--	N.C.	--
15	O	DIP_ON	B	31	I	Di4	A	47	O	DONA	B	63	--	N.C.	--
16	--	N.C.	--	32	I	Di5	A	48	--	N.C.	--	64	--	N.C.	--

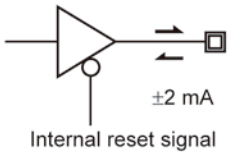
Type-A Pull-up register Schmitt input



V_{t+} max = 0.8 × V_{DD}
V_{t-} min = 0.2 × V_{DD}
ΔV_t min = 0.6V

Rpu (Pull-up register) Typ: 100 KΩ (30 KΩ to 300 KΩ: V_{DD} = 3.0 V, V_I = Vss)

Type-B Push-pull output

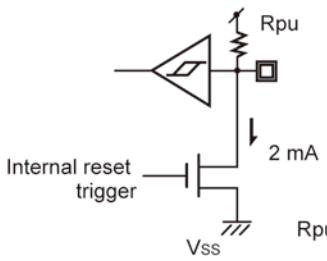


V_{OH} min = 2.4 V (V_{DD} = 3.0 V, I_{OH} = -2 mA)
V_{OL} max = 0.4 V (V_{DD} = 3.0 V, I_{OL} = 2 mA)

I_{OH} max = -2 mA
I_{OL} max = 2 mA

The Type B output pin is in a high impedance state during hardware reset.
For user application devices for which this state is inappropriate, connect to the pin either pull-down resistance or pull-up resistance that can ensure initial levels suitable for the user application.

Type-C Pull-up register Schmitt input
Open drain output

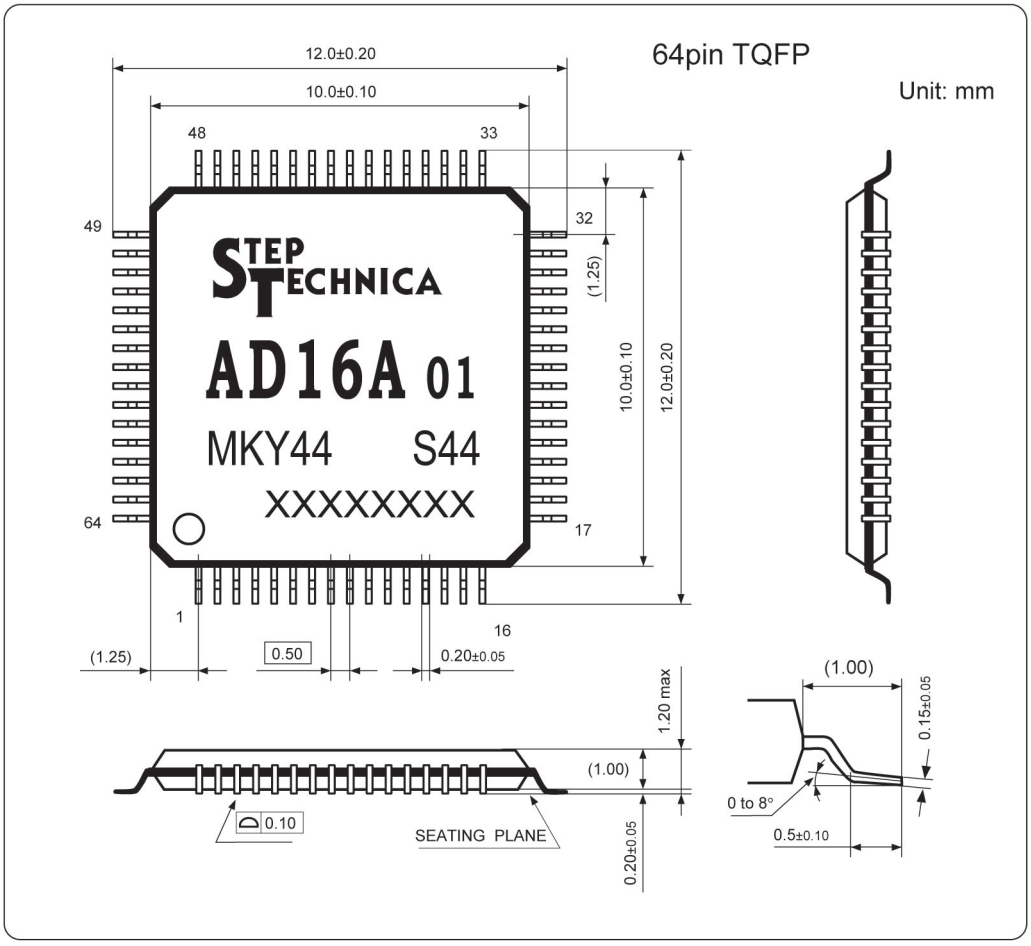


V_{t+} max = 0.8 × V_{DD}
V_{t-} min = 0.2 × V_{DD}
ΔV_t min = 0.6V

V_{OL} max = 0.4 V (V_{DD} = 3.0 V, I_{OL} = 2 mA)
I_{OL} max = 2 mA

Rpu (Pull-up register) Typ: 100 KΩ (30 KΩ to 300 KΩ: V_{DD} = 3.0 V, V_I = V_{SS})

■ Package Dimensions



Revision History

Version	Data	Page	Contents
1.1E	NOV 2013		Issued the first edition
1.2E	AUG 2018	P9	Corrected #Reset signal I/O type.
		P12	Corrected the rated values of Type-A and Type-C
		ALL	Corrected typos of entire document
1.3E	OCT 2020	P9	Added the functional description for XTAL4i and XTAL4o
1.4E	JAN 2024	P14	Change of address

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Related Manuals:

CUnet Introduction Guide		**STD_CUSTU_Vx.xE**
CUnet Technical Guide		**STD_CUTGN_Vx.xE**
CUnet IC	**MKY43 User's Manual**	**STD_CU43_Vx.xE**
CUnet I/O- IC	**MKY46 User's Manual**	**STD_CU46_Vx.xE**
CUnet HUB- IC	**MKY02 User's Manual**	**STD_CUH02_Vx.xE**

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