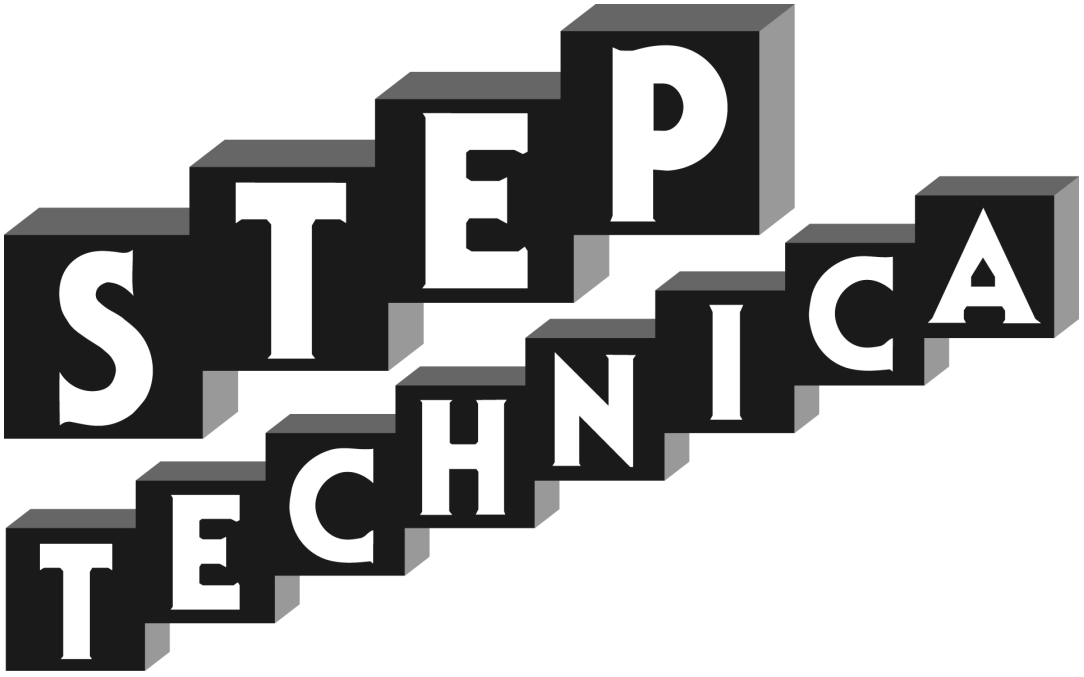
STD-HLS35_V6.2E

STEP TECHNICA CO.,LTD.



Hi-speed Link System Satellite IC

MKY35

User's Manual

Note

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Preface

This manual describes the MKY35, or a kind of satellite IC in the Hi-speed Link System.
Be sure to read ***"Hi-speed Link System Introduction Guide"*** before understanding this manual and the MKY35.
In this manual, the Hi-speed Link System is abbreviated as "HLS".

● **Target Readers**

This manual is for:

- Those who first build an HLS
- Those who first use StepTechnica's various ICs to build an HLS

● **Prerequisites**

This manual assumes that you are familiar with:

- Network technology
- Semiconductor products (especially microcontrollers and memory)

● **Related Manuals**

- Hi-speed Link System Introduction Guide
- Hi-speed Link System Technical Guide

[Caution]

- **To users with *"Hi-speed Link System User's Manual"* up to "Fourth Edition" released before March, 2001**

  Some terms in this manual have been changed to conform to International Standards.

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This chapter describes the outline of the MKY35 in the Hi-speed Link System (HLS).

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This chapter describes the outline of the MKY35 in the Hi-speed Link System (HLS).

1.1 Role of Satellite IC and Relationship with MKY35

MKY35 is a kind of satellite IC that constitutes the HLS. Be sure to read ***"Hi-speed Link System Introduction Guide"*** before understanding the MKY35 and this manual.
The MKY35 must be assigned individual satellite addresses (SAs).

The satellite IC in HLS returns a response packet (RP) in response to a command packet (CP), which matches a SA, from the center IC. This causes the state of the input pin (Di) of the satellite IC to be copied directly to the Di area of memory in the center IC. The CP issued from the center IC is embedded with one data item arranged in the Do area of memory in the center IC.

The satellite IC in HLS outputs data in the CP to the output pin (Do) of the satellite IC each time it receives a CP matching the SA. The center IC periodically transmits a CP and receives a RP to continue scanning the satellite IC. This series of continuous operation links the state of the input pin (Di) of the satellite IC with data in the Di area of memory in the center IC, and data in the Do area of memory in the center IC with the state of the output pin (Do) of the satellite IC. The Di and Do areas of memory in the center IC are arranged corresponding to each SA that must be set to the satellite IC (Fig. 1.1).

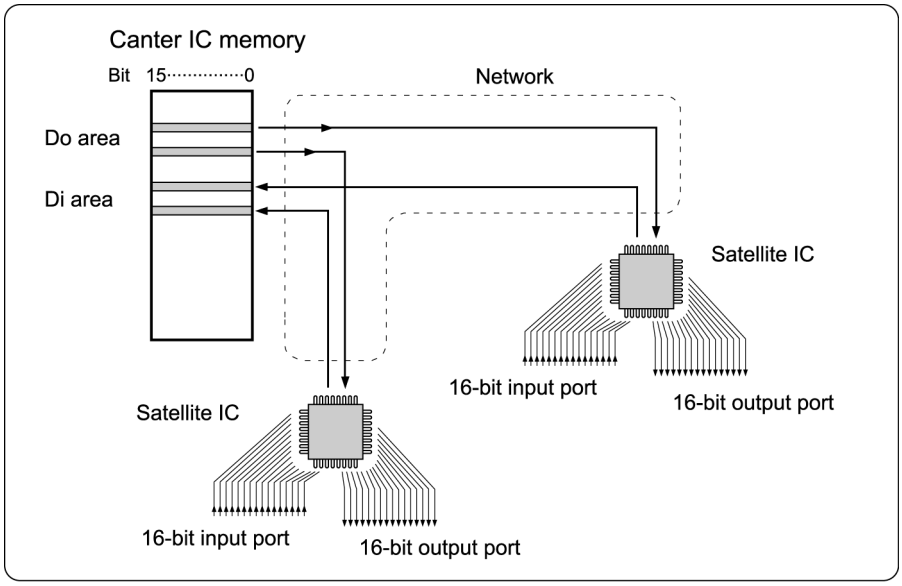

Fig. 1.1 Role of Satellite IC

The MKY35 is a miniaturized package satellite IC with 32 I/O ports—16 for input (Di) and 16 for output (Do). The package has 16 input and output pins that can be connected to any of the 32 input and output (I/O) ports. In addition to these input (Di) and output (Do) pins, the MKY35 has some expanded functions for embedding in various user systems.

1.2 Internal Structure

The MKY35 has a standard satellite IC core and also has 16 Io pins (Io0 to Io15) and three IOS (IO Select) pins (Fig. 1.2).
The standard satellite IC core has 16 internal input terminals (Di) and 16 internal output terminals (Do), but these terminals are not connected directly to the external pins. These input and output terminals are connected to the Io pins (Io0 to Io15), or external pins by setting three IO select (IOS) pins.

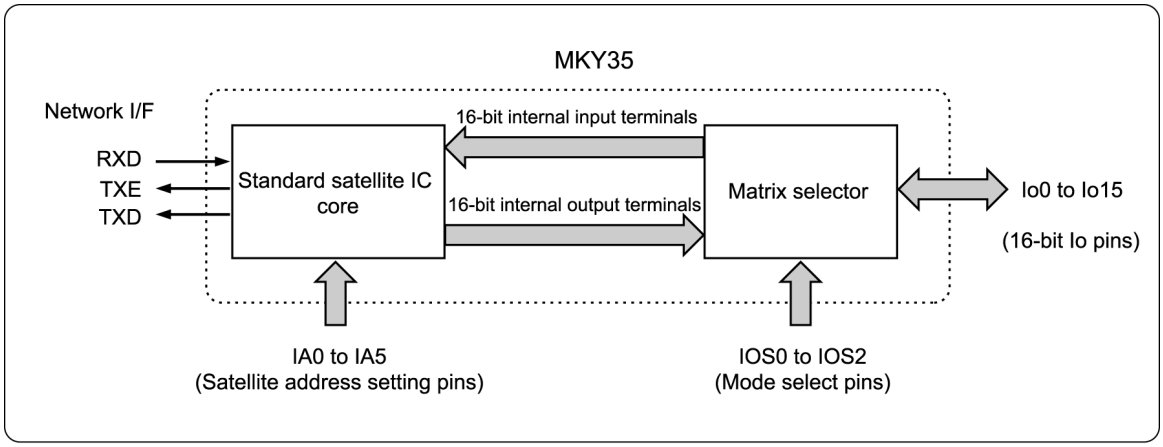

Fig. 1.2 Internal Structure of MKY35

Reference For details of the connection between the Io pins (Io0 to Io15) and internal input or output terminals by setting the IOS pins, refer to ***"3.5 Selecting Operation Mode of MKY35"***.

1.3 Procedure for Operating MKY35

The MKY35 is a passive IC and it is operated by remote control from center ICs. In an HLS where a center IC continues to scan, the user system (for access to center ICs) to use the MKY35 is very simple.

(1) The user system just writes data to memory in the center IC when it wants to change the state of the internal output terminals (Do0 to Do15) of the MKY35. For example, when a relay is connected to the Io pin to which internal output terminals (Do0 to Do15) of the MKY35 is connected, the user system program simply writes data to memory in the center IC only when it wants to turn the relay "on" or "off".

(2) The user system simply reads memory in the center IC when it wants to obtain the state of the internal input terminals (Di0 to Di15) of the MKY35. For example, when a sensor is connected to the Io pin to which the internal input terminals (Di0 to Di15) of the MKY35 is connected, the user system program can obtain the state of the sensor by reading memory in the center IC.

If the center IC can issue multiple commands (0 to FH), the MKY35 responds to command "0", which is a basic function of the HLS. Handle the expanded functions of the MKY35 using the command "0".

Caution Even if the MKY35 receives a command packet (CP) other than command "0", it has no operational function. In this case, the MKY35 returns a response packet (RP) containing data at 0000H.

1.4 MKY35 Response Time

The main feature of the HLS where a center IC continues to scan, is that constancy and real-timeness are assured. The time required to link data in memory in the center IC with the states of the internal input terminal (Di) and internal output terminal (Do) of the MKY35 essentially matches the scan time of the HLS, which is very fast.

For example, in a user system that must detect the exact position of each box on a belt conveyor, if four MKY35 with 16 Io pins (Io0 to Io15) set to "input" are connected to the center IC and position detection sensors are connected to the Io pins of all MKY35s, the state of 64 sensors (16 sensors × 4 MKY35) is stored to memory in the center IC with a scan time intervals of 60.7 μs (12 Mbps: full duplex), keeping data up-to-date. This speed remains unchanged even if the farthest MKY35 is 100-m distant. Even if the position detection sensors are placed at every 5 cm, they can detect the position of every box on the belt conveyor without mistakes even when the conveyor runs at 823 m/s (>2900 km/h).

For details of the scan time, refer to ***"Scan Time"*** in the ***"User's Manual"*** for the center IC connecting the MKY35.

1.5 Features of MKY35

This section describes the basic and the expanded functions of the MKY35.

1.5.1 Features of Basic Functions of MKY35 as Satellite IC in HLS

(1) Miniaturized satellite IC
(2) Has 16 Io pins (Io0 to Io15) for "input" or "output".
(3) Supports baud rates of 12, 6, and 3 Mbps
(4) Supports full- and half-duplex modes
(5) Has six pins to set satellite addresses (SA) for any one of 63 terminals at 01H to 3FH
(6) Operates on 5.0-V single power supply and available in 0.5 mm pitch, 48 pins, TQFP

1.5.2 Expanded Functions

(1) Has pin that outputs scan response signals
(2) Has CLR pin that sets internal output terminals (Do0 to Do15) Low
(3) Has strobe output pins that indicate when to update internal output terminals (Do0 to Do15) and a timing to receive internal input terminals (Di0 to Di15)
The user can design peripheral circuits based on each update timing
(4) Can set handshake to ensure link with center IC
(5) Has two types of PWM (Pulse Width Modulation) modes to control current and DC motor

Chapter 2 MKY35 Hardware

This chapter describes the MKY35 hardware, such as pin assignment, pin functions, and I/O circuit types.

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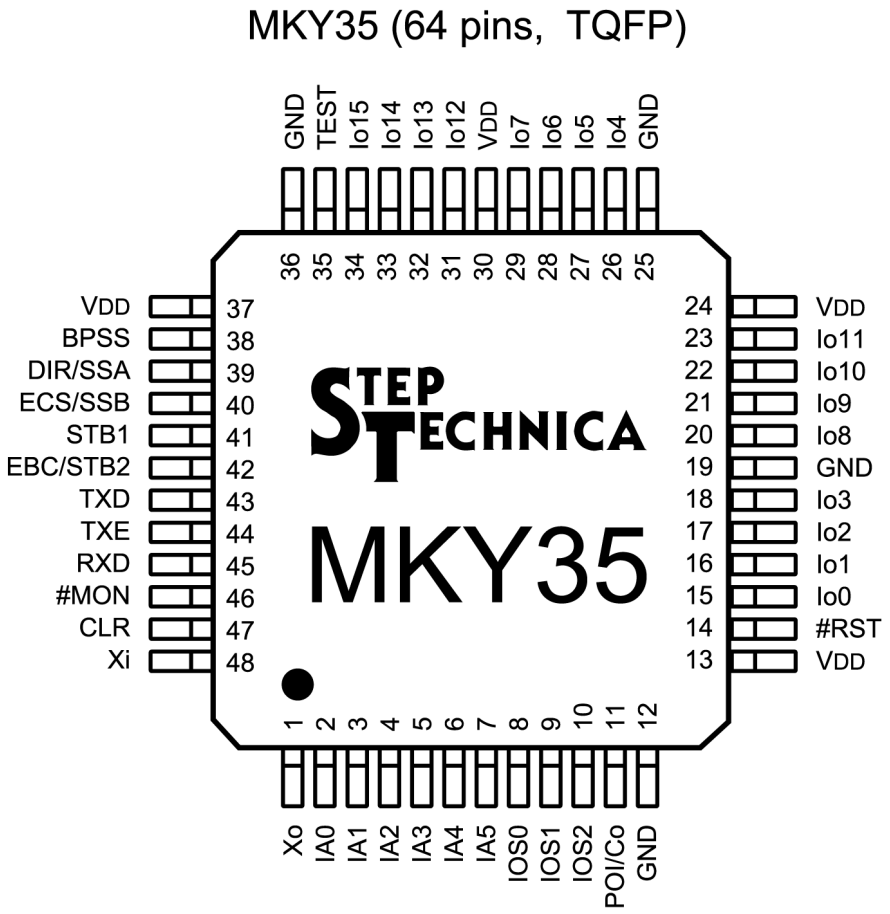
Figure 2.1 shows the MKY35 pin assignment.



Note: Pins prefixed with # are negative logic (active Low).

Fig. 2.1 MKY35 Pin Assignment

Table 2-1 lists the pin functions of the MKY35.

Table 2-1 Pin Functions of MKY35

Pin name	Pin No.	Logic	I/O	Function
Xo	1	Positive	O	Pin that connects oscillator
IA0 to IA5	2 to 7	Positive	I	Input pins that sets satellite addresses Set the hexadecimal values 1 to 63 (01H to 3FH) in positive logic, assuming a High level as 1. The IA5 pin corresponds to MSB. (When these pins are open, they are recognized as Low-level inputs by the internal pull-down resistor.)
IOS0 to IOS2	8 to 10	Positive	I	Input pins that selects MKY35 operation mode Set hexadecimal values 0 to 7 (0H to 7H). The IOS2 pin corresponds to MSB. Be sure to set these three pins High or Low. (When the pins are open, they are recognized as Low-level inputs by the internal pull-down resistor.)
Co/POI	11	Positive	O/I	O/I pin that functions as Co pin (output pin) when any of the IO modes 1 to 6 is selected by the IOS0 to IOS2 pins. It outputs the MKY35 driving clock. O/I pin that functions as POI pin (input pin) when the PWM mode 1 or 2 is selected by the IOS0 to IOS2 pins. The POI pin is an input pin. Connect POI signal supplied to the PWM circuit to the POI pin. Be sure to set this pin High or Low when the PWM mode 1 or 2 is selected by the IOS0 to IOS2 pins.
#RST	14	Negative	I	MKY35 Hardware reset input pin Keep this pin Low for 10 or more clocks of the Xi pin frequency right after power-on or when resetting hardware intentionally.
Io0 to Io15	15 to 18 26 to 29 20 to 23 31 to 34	Positive	I/O	16-bit general-purpose I/O pins The input/output and function are set based on the setting of the IOS0 to IOS2 pins.
TEST	35	Positive	I	Be sure to connect this pin to GND (manufacturer test pin)
BPSS	38	Positive	I	Input pin that selects driving clock (When this pin is open, it is recognized as a Low-level input by the internal pull-down resistor.)
SSA/DIR	39	Positive	I	Input pin that functions as SSA pin when any of the IO modes 1 to 6 is selected by the IOS0 to IOS2 pins. Set a High level or Low level to select the strobe signal functions to the SSA pin. Input pin that functions as DIR pin when the PWM mode 1 or 2 is selected by the IOS0 to IOS2 pins. Connect DIR signal supplied to the PWM circuit to the DIR pin. When this pin is open, it is recognized as a Low-level input by the internal pull-down resistor.

(Continue)

Table 2-1 Pin Functions of MKY35 (Continued)

Pin name	Pin No.	Logic	I/O	Function
SSB/ECS	40	Positive	I	Input pin that functions as SSB pin when any of the IO modes 1 to 6 is selected by the IOS0 to IOS2 pins. Set a High level or Low level to select the strobe signal functions to the SSB pin. Input pin that functions as ECS pin when the PWM mode 1 or 2 is selected by the IOS0 to IOS2 pins. Connect ECS signal supplied to the PWM circuit to the DIR pin. When this pin is open, it is recognized as a Low-level input by the internal pull-down resistor.
STB1	41	Positive	O	Output pin that outputs High-level pulse of strobe signals indicating timing to update state of internal output terminal when command packet received correctly from center IC
STB2/EBC	42	Positive	O/I	O/I pin that functions as STB2 pin when any of the IO modes 1 to 6 is selected by the IOS0 to IOS2 pins. STB2 pin outputs High-level pulse of strobe signals indicating timing to input state of Io pin into internal input terminals. O/I pin that functions as EBC pin (input pin) when any of the PWM mode 1 or 2 is selected by the IOS0 to IOS2 pins. Connect EBC signal supplied to the PWM circuit to the EBC pin. Be sure to set this pin High or Low when the PWM mode 1 or 2 is selected by the IOS0 to IOS2 pins.
TXD	43	Positive	O/Z	Pin that outputs response packet to center IC Connect this pin to the drive input pin of a driver. This pin goes high-impedance when the TXE pin is Low.
TXE	44	Positive	O	Output pin that goes High while outputting response packet to center IC Connect this pin to the enable input pin of a driver.
RXD	45	Positive	I	Input pin that inputs command packet sent from center IC Connect this pin to the output pin of a receiver.
#MON	46	Negative	O	Output pin that outputs scan response state of MKY35 Low level is output when a correct scan response is made.
CLR	47	Positive	I	Input pin that forcibly set all internal output terminals Low Usually, keep this pin Low. (When this pin is open, it is recognized as a Low-level input by the internal pull-down resistor.)
Xi	48	Positive	I	Pin for connection of oscillator or generated clock
V_{DD}	13, 24 30, 37	---	---	Power pin connected to 5.0 V
GND	12, 19 25, 36	---	---	Power pin connected to 0 V

Note: Pins prefixed with # are negative logic (active Low).

Table 2-2 and Figure 2.2 shows the electrical ratings of the MKY35 pins.

Table 2-2 Electrical Ratings of MKY35

(#: Negative logic)

No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type
1	O	Xo	--	13	--	VDD	--	25	--	GND	--	37	--	VDD	--
2	I	IA0	A	14	I	#RST	C	26	I/O	Io4	F	38	I	BPSS	A
3	I	IA1	A	15	I/O	Io0	F	27	I/O	Io5	F	39	I	SSA/DIR	A
4	I	IA2	A	16	I/O	Io1	F	28	I/O	Io6	F	40	I	SSB/ECS	A
5	I	IA3	A	17	I/O	Io2	F	29	I/O	Io7	F	41	O	STB1	H
6	I	IA4	A	18	I/O	Io3	F	30	--	VDD	--	42	O/I	STB2/EBC	G
7	I	IA5	A	19	--	GND	--	31	I/O	Io12	F	43	O/Z	TXD	I
8	I	IOS0	A	20	I/O	Io8	F	32	I/O	Io13	F	44	O	TXE	H
9	I	IOS1	A	21	I/O	Io9	F	33	I/O	Io14	F	45	I	RXD	D
10	I	IOS2	A	22	I/O	Io10	F	34	I/O	Io15	F	46	O	#MON	J
11	O/I	Co/POI	E	23	I/O	Io11	F	35	I	TEST	B	47	I	CLR	A
12	--	GND	--	24	--	VDD	--	36	--	GND	--	48	I	Xi	--

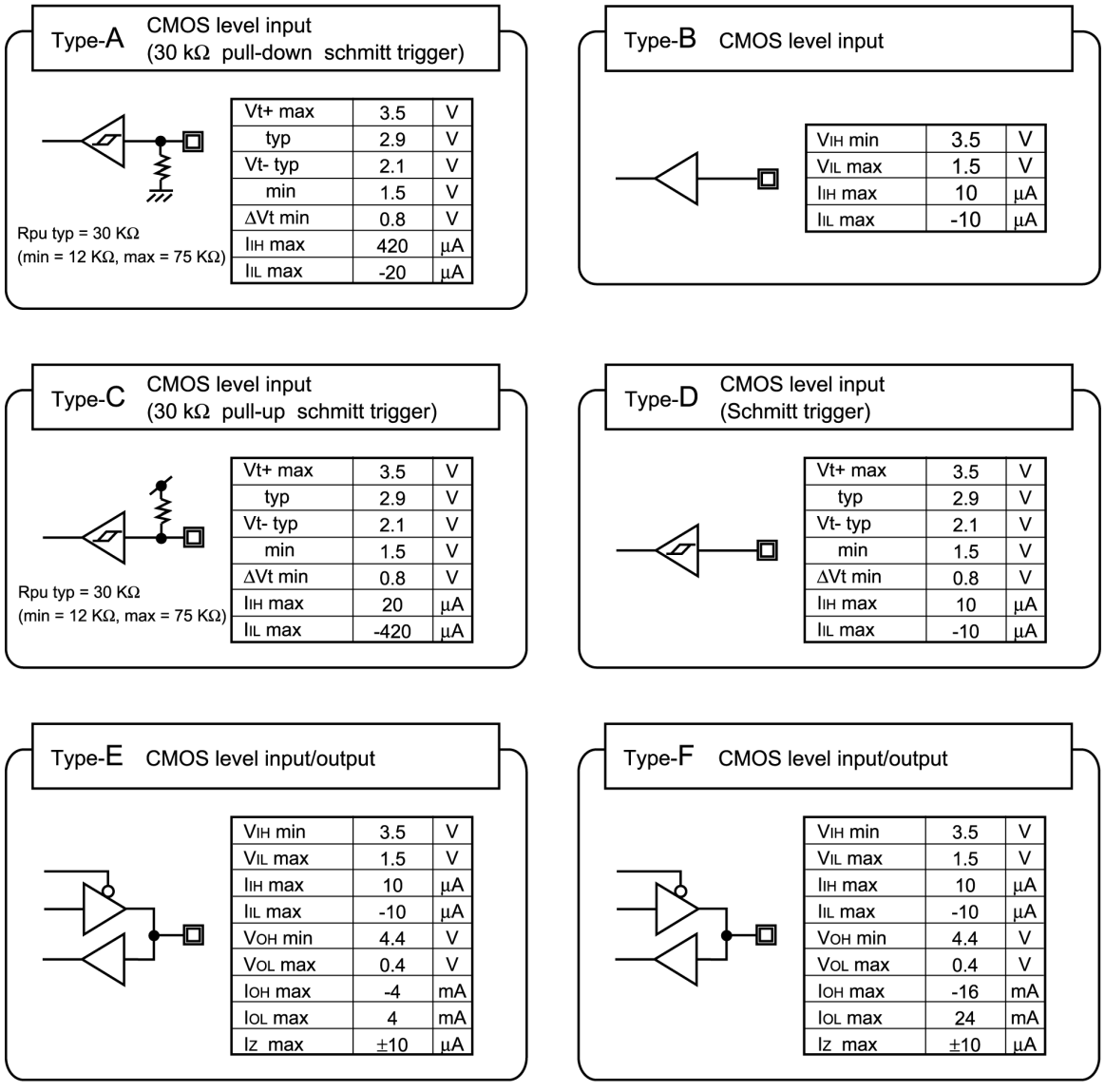


Fig. 2.2 Pin Electrical Characteristics in I/O Circuit Types of MKY35

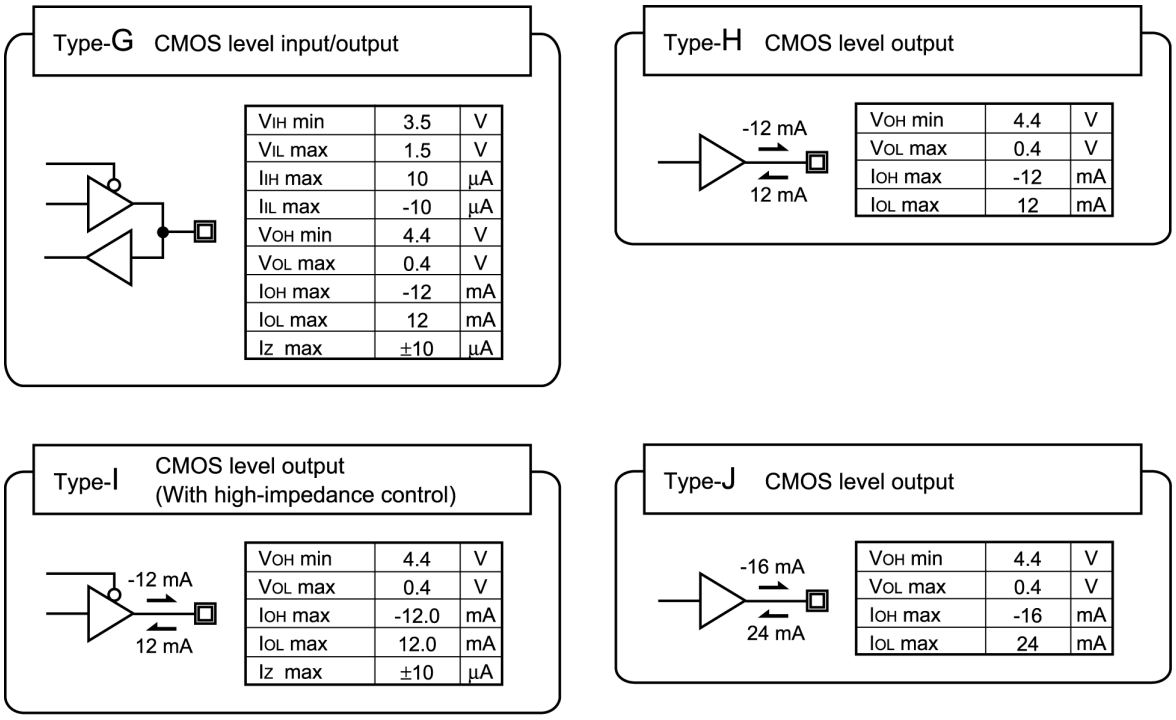


Fig. 2.2 Pin Electrical Characteristics in I/O Circuit Types of MKY35

Chapter 3 Connecting Basic Functions of MKY35

This chapter describes the pin functions and connections required to operate the basic functions of the MKY35.

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3.1 Driving Clock

This section describes the MKY35 driving clock.

3.1.1 Self-generation of Driving Clock

The MKY35 can be connected to an oscillator to self-generate a driving clock. In this case, connect the oscillator to the Xi pin (pin 48) and Xo pin (pin 1). The frequency of driving clock to be generated must be four or eight times greater than the baud rate. For example, if the baud rate is 6 Mbps, the frequency of the driving clock is 24 or 48 MHz. If the driving clock is generated correctly and the MKY35 is in IO mode 1 to 6, the user can find that the Co (Clock out) pin (pin 11) outputs the clock. This clock is output from the Co pin when the BPSS (BPS Select) pin (pin 38) is Low and while the hardware reset is activated.
Place the oscillator and auxiliary component to be connected to the Xi and Xo pins near the MKY35. Supported oscillators include crystal and ceramic types. Select an appropriate value for the additional capacitance depending on the oscillator types and manufacturers (Fig. 3.1).

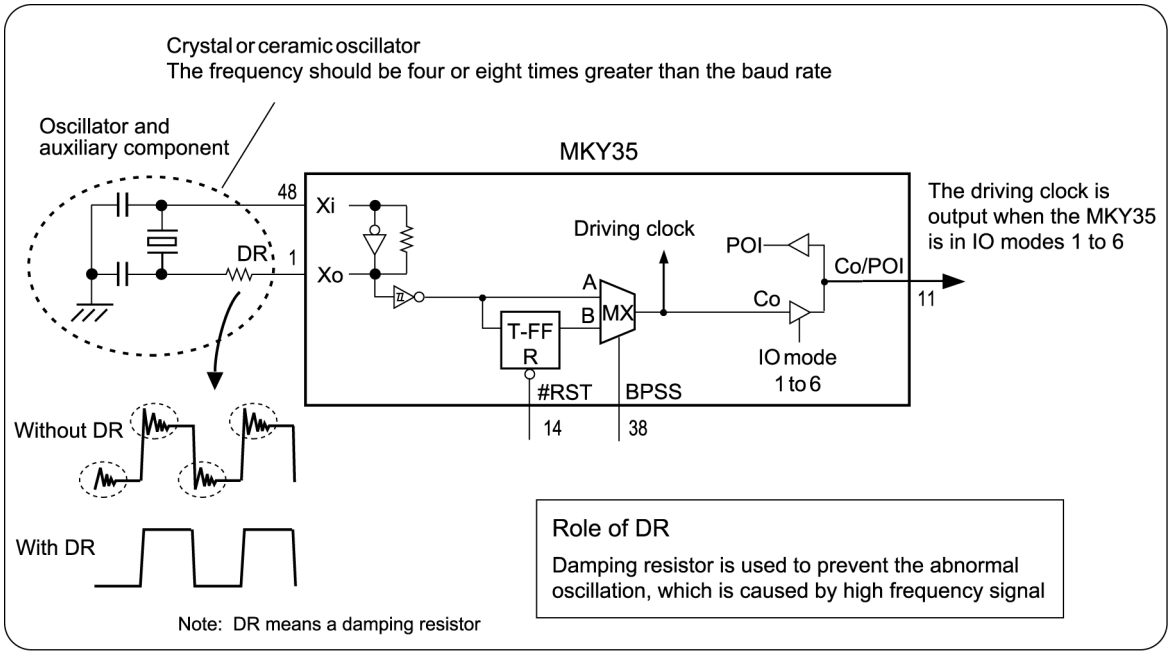

Fig. 3.1 Clock Relationship Diagram for MKY35

Caution

(1) The MKY35 oscillation frequency ranges from 20 MHz to 50 MHz. If the driving clock frequency outside this range is required, use the generated clock described in ***"3.1.2 Supplying Generated Driving clock"***.

(2) Some oscillator types may need to be inserted a dumping resistor (DR) between the Xo and oscillator.

(3) The allowable oscillating frequency accuracy is within ±5% for a frequency four times the baud rate. If the frequency accuracy is low, the allowable length of the network cable to the center IC may be short. To prevent this, StepTechnica recommends a crystal oscillator be used to maintain the accuracy within ±1%.

(4) To recognize the oscillating state and measure the oscillating frequencies, use the CO pin with the MKY35 being in IO mode 1 to 6.

Reference

StepTechnica provides some technical information, such as an appropriate capacitance for the oscillator, how to stabilize oscillation. For more information, visit our Web site at **www.steptechnica.com/**

3.1.2 Supplying Generated Driving Clock

An oscillator-generated external clock can be supplied directly to the MKY35 and used as the driving clock. In this case, supply the external clock to the Xi pin (pin 48) of the MKY35 and leave Xo pin (pin 1) open. The specifications for direct supplying the external clock are as follows:

(1) The upper frequency is 50 MHz and a lower frequency is not provided.
(2) V_{IH} = min. 3.5 V, V_{IL} = max. 1.5 V
(3) Clock with a signal rise and fall times of 20 ns or less
(4) Clock with a minimum High-level or Low-level time of 5 ns or more
(5) Clock with jitter component of:
- Within 250 ps when input frequency is 25 MHz or more
- Within 500 ps when input frequency is less than 25 MHz

(6) Frequency accuracy of 1000 ppm (±0.1%) or better

Reference

For a commonly-used oscillator, there is no problem with clock output by the values above in (2) to (6).

3.1.3 Selecting Driving Clock

When the BPSS (BPS Select) pin (pin 38) is Low, the driving clock for the MKY35 is either self-generated clock or external clock. On the other hand, when the BPSS (BPS Select) pin (pin 38) is High, the driving clock is a two-divided clock into which the MKY35 dividing circuit divides the frequency of the self-generated clock or the external clock.
Set the BPSS pin and the frequency of the self-generated or external clock so that they will match the baud rate to be set to the HLS center IC connecting the MKY35 (Table 3-1).

Table 3-1 Correspondence between Driving Clock and Baud Rate

	BPSS = Low level		BPSS = High level	
Frequency at Xi pin	Driving clock	Baud rate	Driving clock	Baud rate
48 MHz	48 MHz	12 Mbps	24 MHz	6 Mbps
24 MHz	24 MHz	6 Mbps	12 MHz	3 Mbps
12 MHz	12 MHz	3 Mbps	6 MHz	1.5 Mbps

3.1.4 Checking Driving clock

The Co (Clock out) pin (pin 11) of the MKY35 is connected like an internal equivalent circuit shown in Figure 3.1. When the MKY35 is in IO mode 1 to 6, the driving clock can be checked by the Co pin. The driving clock output from the Co pin can be used for purposes other than checking the driving clock. However, as shown in Figure 3.1, while a hardware reset is activated with the BPSS pin being High, the output level of Co pin keeps Low and no clock is output.

For the MKY35 operation mode, refer to ***"3.5 Selecting Operation Mode of MKY35"*** and ***"4.3 PWM Modes"***.

3.2 Hardware Reset

When a Low level is input to the #RST (ReSeT) pin (pin 14), the MKY35 is hardware-reset. If a period in which the Low-level signal has been input is less than "one clock", the signal is ignored to prevent malfunction. To reset the MKY35 completely, the #RST pin must be kept Low for "10 or more clock" while supplying a driving clock. The #RST pin is connected to an internal Schmitt-type input buffer, so a constant-rise-time circuit can be connected directly at power-on (Fig. 3.2).

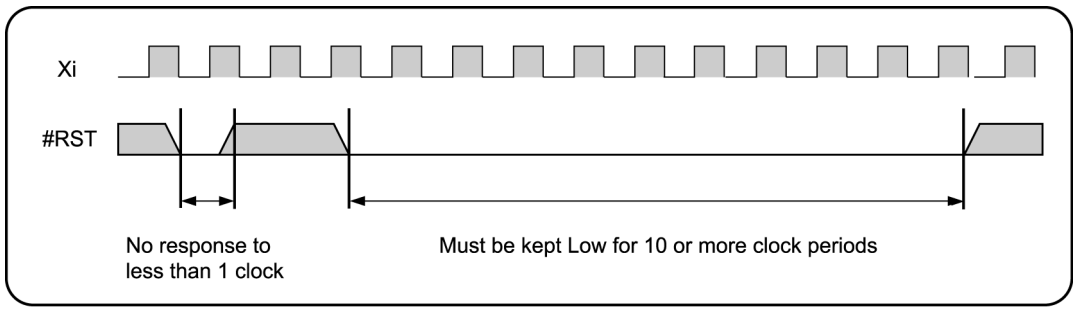

Fig. 3.2 Hardware Reset

Caution Design the circuit so that a hardware reset is surely activated immediately after MKY35 power-on.

3.3 Setting Satellite Addresses

The MKY35 has six satellite address (SA) setting pins (IA0 to IA5: Input Addresses 0 to 5). Individual satellite addresses (SA) must be assigned to each satellite IC when using the HLS. To set the SA values to the MKY35, use hexadecimal numbers from 01H to 3FH (addresses 1 to 63) assuming a High level is input to IA0 to IA5 (pins 2 to 7) as "1" and a Low level is input as "0". The most significant bit is IA5 (pin 7). These SA settings correspond to the memory addresses in each area in the center IC.

- **Example 1: The state of the internal input terminal (Di) of the MKY35 at SA = 1 (01H) is stored at address 02H in the Di area of memory in the center IC.**
- **Example 2: The state of the internal input terminal (Di) of the MKY35 at SA = 63 (3FH) is stored at address 7EH in the Di area of memory in the center IC.**

Reference There are no limitations on physical network arrangement, such as setting the SA values in the order in which they are closer to the center IC. If the center IC has two input pins (RXD1 and RXD2), there are no rules, such as which pin (network) the MKY35 in which specific SA values are set is connected to.

Caution The different SA values must be set to all satellite ICs connected to center ICs. The SA value cannot be set to 00H. Even if the SA value of 00H is set to a satellite IC by mistake, the system is not adversely affected but the satellite IC is not scanned by the center IC.

3.4 Connecting Network Interface

The network interface (network I/F) pins of the MKY35 consist of RXD (pin 45), TXE (pin 44), and TXD (pin 43).

3.4.1 Details of RXD, TXE, and TXD Pins

In the MKY35, the RXD pin inputs a command packet (CP) from the center IC. Connect the TRX (driver/ receiver components) in the network so that a serial pattern signal for the command packet (CP) transmitted from the center IC will be input to the RXD pin.

If the address of the received CP matches the SA set by IA0 to IA5, the MKY35 immediately returns a response packet (RP) to the center IC. The TXE pin goes High while the MKY35 sends the RP. When the TXE pin goes high, design the TRX so that the enable pin of the TRX is activated, thereby enabling the serial pattern signal for the RP output from the TXD pin to be transmitted to the network.

The TXD pin of the MKY35 outputs High-level or Low-level pulses comprising the RP during sending the RP. The TXD pin goes high-impedance when the TXE pin is Low (the RP is not transmitted) and a hardware reset is activated, enabling wired OR connection when implementing multiple MKY35s on the same circuit board. Drive input pins of the TRX driver are pulled up within the driver, which allows the TXD pin to be connected to the drive input pin directly. When connecting the TXD pin to the drive input pin of a driver not pulled up internally, pull it up (or down).

When the hardware reset is activated, the TXE pin of the MKY35 keeps the last level. The pin always goes Low whenever the hardware reset is canceled.

When the HLS operates in half-duplex mode, the signal output from the TXD pin of the MKY35 may be input directly to the RXD pin while the MKY35 is returning the RP. The MKY35 is designed not to input data when the TXE pin is High, so there is no problem.

3.4.2 Recommended Network Connection

Figure 3.3 shows the recommended network connection. The TRX (driver/receiver components) consists of an RS485-based driver/receiver (LSI driven at 5.0 V) and pulse transformer. Recommended network cables include Ethernet LAN network cables (10BASE-T, Category 3 or higher) and shielded network cables. When operating the HLS, full-duplex mode requires two twisted-pair cables, and half-duplex requires one twisted-pair cable (Fig. 3.3).

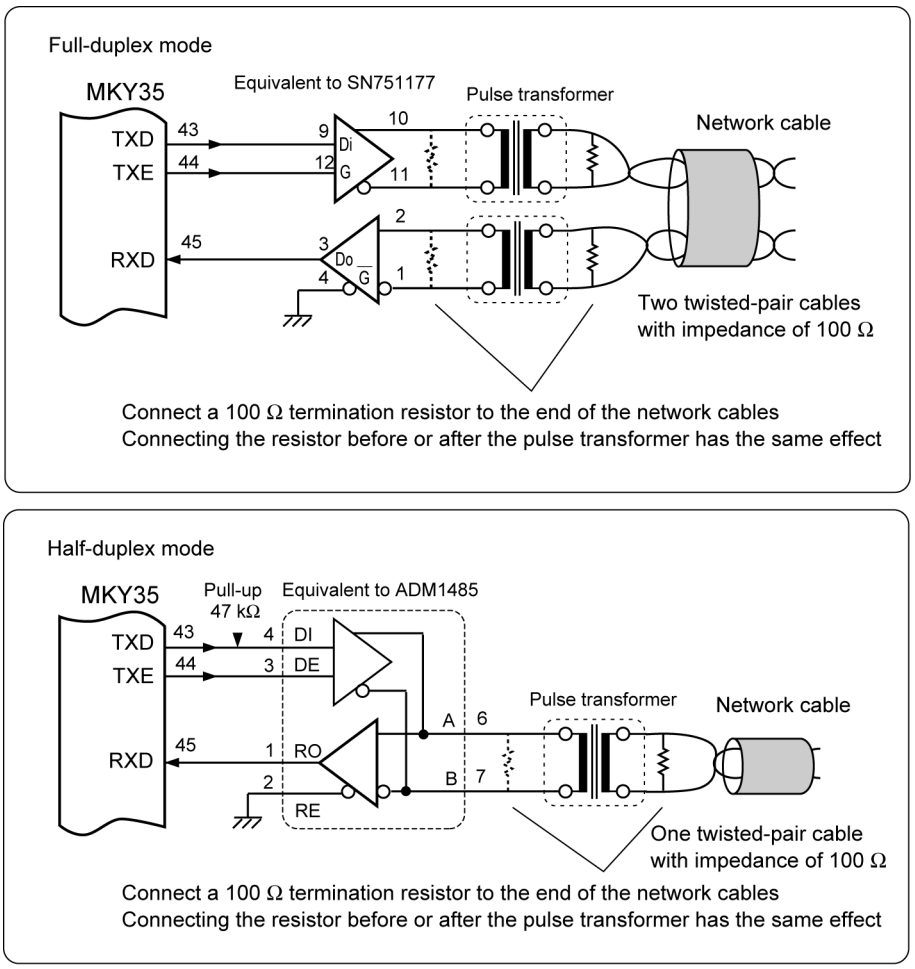

Fig. 3.3 Recommended Network Connection

Caution The TXD pin of the MKY35 goes high-impedance while it does not send RP. When using driver components that does not allow the driver input to go high-impedance, connect a pull-up or pull-down resistor to the connection line between the TXD pin and driver input.

Reference The High-level signal of the network interface output to the TXE pin (pin 44) can be used to detect that the center IC is scanning. It can also be used to check the operation of the user system using the HLS and measure the response speed.

Background information to help build network cables is described in ***"Hi-speed Link System Technical Guide"***. For more information about how to select components or to get recommended components, visit our Web site at **www.steptechnica.com/**

3.5 Selecting Operation Mode of MKY35

The MKY35 operation mode can be selected by three IOS (IO Select) pins. The MKY35 has 16 Io pins (Io0 to Io15). These pins can be used for “input” or “output” by setting the IOS pins.

Caution

The user can change the operation mode even during operation of the MKY35 by changing the setting of the IOS pins. However, StepTechnica advises the user not to change the setting of the IOS pins during operation because the I/O transition time of active Io pins varies depending on the connection environment including load capacitance, and the output level depends on the operating state.
If the user wants to change the setting of the IOS pins during operation, set the IOS pins carefully to prevent problems, such as the input/output transition of Io pins, and the electronic conflict between output pins, do not occur.

3.5.1 Internal Input Terminal and Internal Output Terminal

The MKY35 has 16-bit internal input terminals (Di0 to Di15) and 16-bit internal output terminals (Do0 to Do15) (Fig. 3.4).

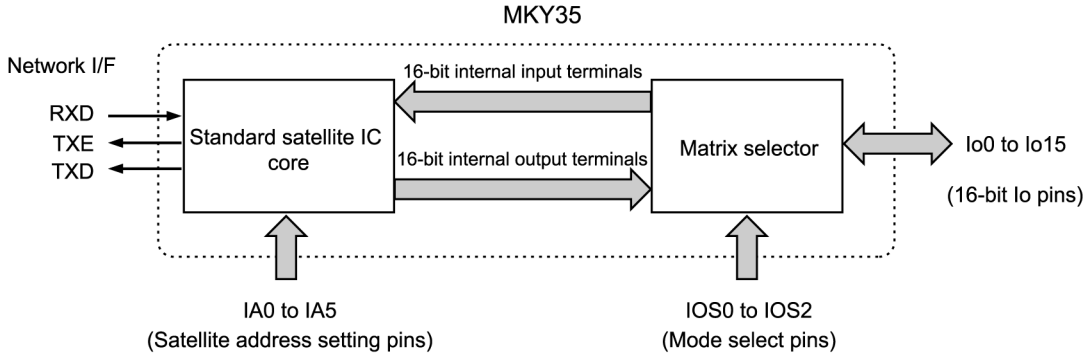

Fig. 3.4 Internal Input Terminal and Internal Output Terminal

The state of the internal input terminals (Di0 to Di15) of the MKY35 is copied to the memory addresses corresponding to the SAs of the Di area in the center IC. When the MKY35 receives a command packet (CP) sent from the center IC correctly and its addresses match the SAs set by the IA0 to IA5 pins, the MKY35 sets data contained in the CP to the 16-bit internal output terminals (Do0 to Do15).

The 16-bit internal output terminals go Low before retaining the above data when a hardware reset is activated. Even after the hardware reset is canceled, the internal output terminals are kept Low until the data is updated. When the CLR pin described in ***“4.1.4 CLR Pin Function”*** becomes activated, the 16-bit internal output terminals also go Low before retaining the data, just as the hardware reset becomes activated.

16 Io pins (Io0 to Io15) are connected to the 16-bit internal input terminals or 16-bit internal output terminals by setting three IOS (IO Select) pins. Connect the internal input terminals that are not connected to the Io pins to GND (0) and leave the internal output terminals that are not connected to the Io pins open.

3.5.2 List of Operation Modes

Table 3-2 lists the MKY35 operation modes.

Table 3-2 MKY35 Operation Modes

IOS2	IOS1	IOS0	Operation mode	Input	Output	Connection of Io0 to Io15 pins, etc.
Lo	Lo	Lo	IO mode 1	16	0	Io0 to Io15 pins → Di0 to Di15
Lo	Lo	Hi	IO mode 2	12	4	Io0 to Io11 pins → Di0 to Di11 Do12 to Do15 → Io12 to Io15
Lo	Hi	Lo	IO mode 3	8	8	Io0 to Io7 pins → Di0 to Di7 Do8 to Do15 → Io8 to Io15
Lo	Hi	Hi	IO mode 4	4	12	Io0 to Io3 pins → Di0 to Di3 Do4 to Do15 → Io4 to Io15
Hi	Lo	Lo	IO mode 5	2	18	Io0 to Io1 pins → Di0 to Di1 Do2 to Do15 → Io2 to Io15
Hi	Lo	Hi	IO mode 6	0	16	Do0 to Do15 → Io0 to Io15
Hi	Hi	Lo	PWM mode 1	8	4	Refer to ***"4.3.1 PWM Mode 1"***
Hi	Hi	Hi	PWM mode 2	4	4	Refer to ***"4.3.3 PWM Mode 2"***

Caution Do not leave the Io pins set to "input" in the user system open. Keep these pins High or Low. For the unused Io pins of those set to "output" in the user system, leave them open.

3.5.3 IO Modes 1 and 2

Figure 3.5 and Figure 3.6 show the internal connections in IO mode 1 and IO mode 2, respectively.

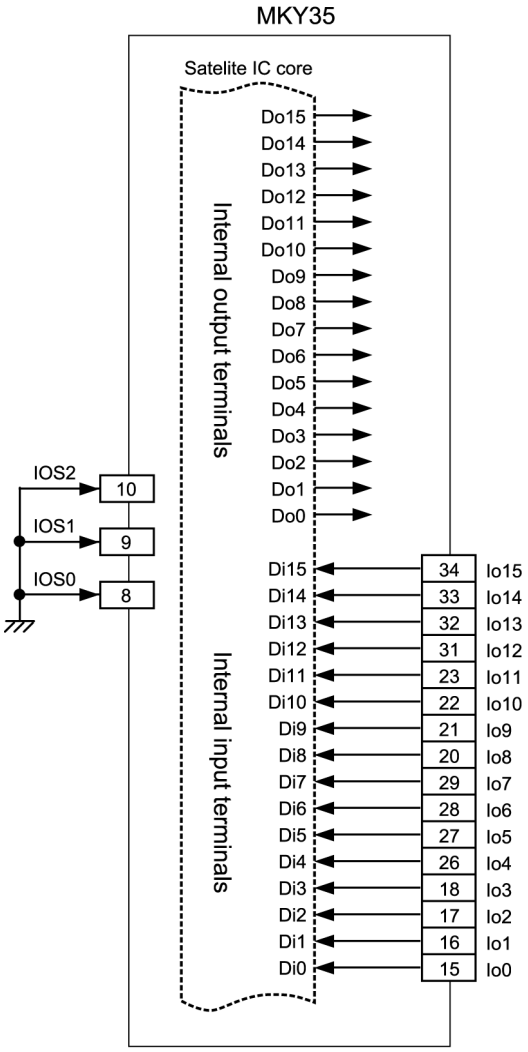

Fig. 3.5 IO Mode 1

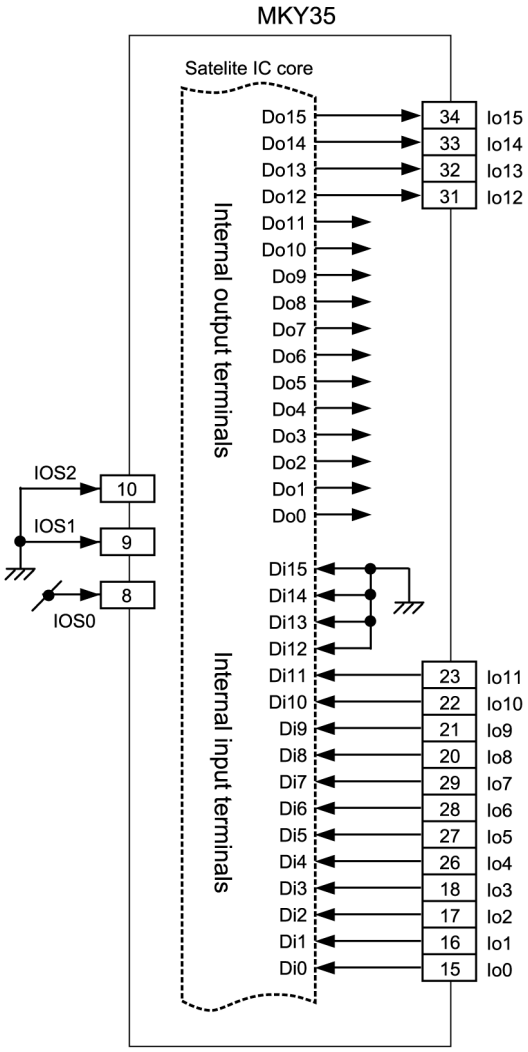

Fig. 3.6 I/O Mode 2

3.5.4 IO Modes 3 and 4

Figure 3.7 and Figure 3.8 show the internal connections in IO mode 3 and IO mode 4, respectively.

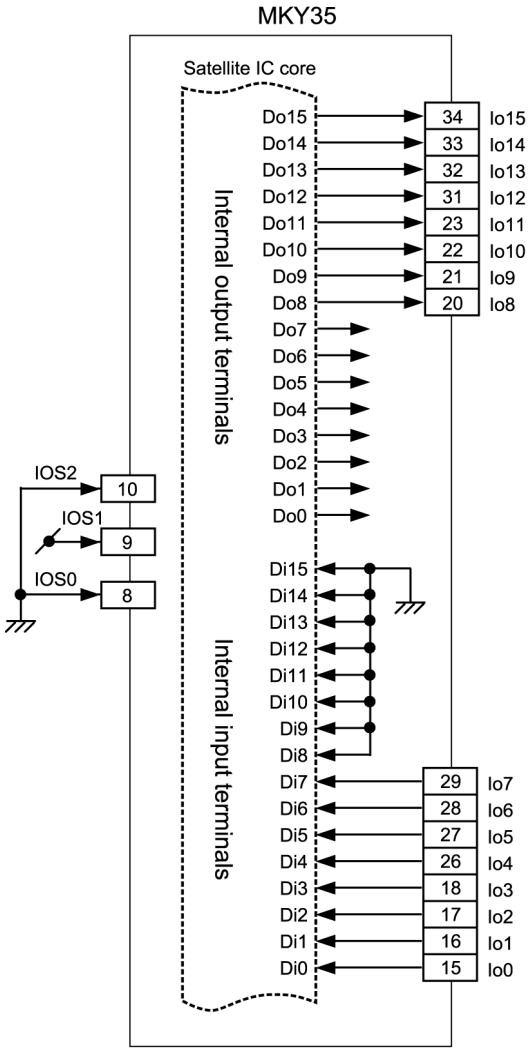

Fig. 3.7 IO Mode 3

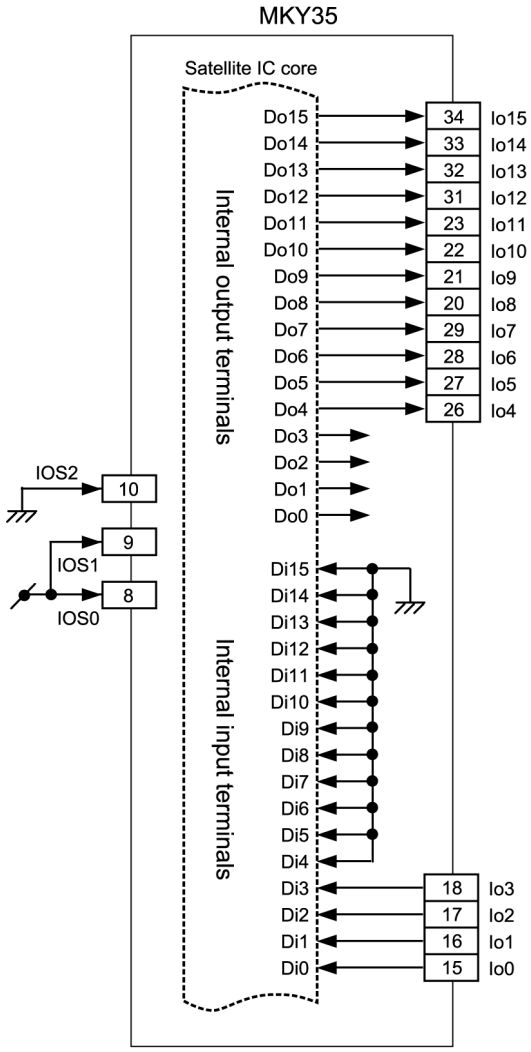

Fig. 3.8 IO Mode 4

3.5.5 IO Modes 5 and 6

Figure 3.9 and Figure 3.10 show the internal connections in IO mode 5 and IO mode 6, respectively.

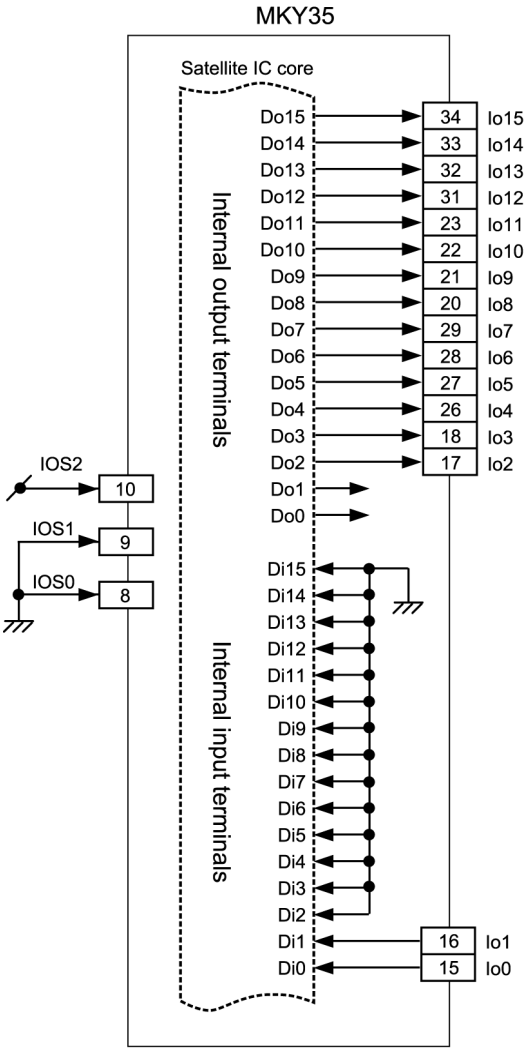

Fig.3.9 I/O Mode 5

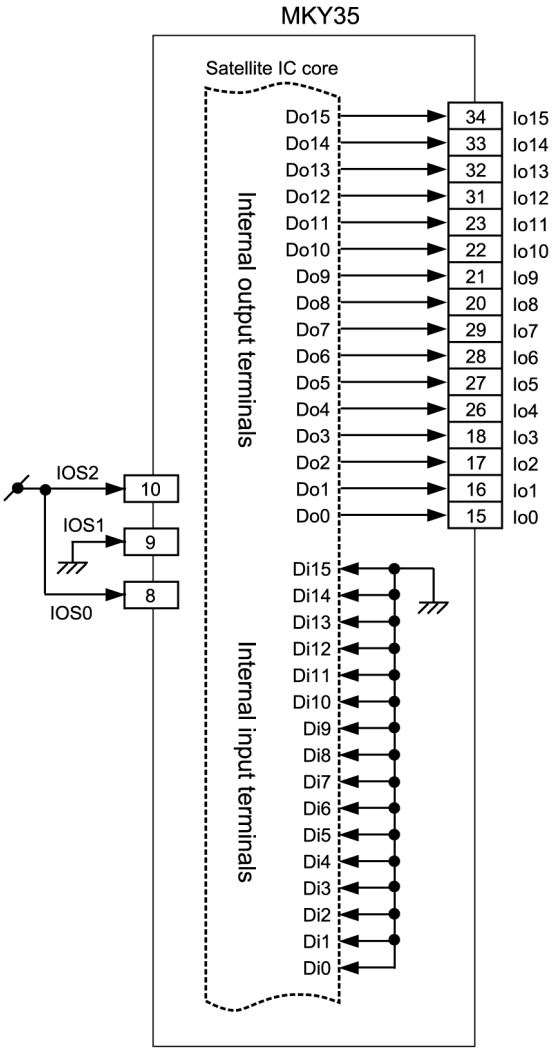

Fig.3.10 I/O Mode 6

3.6 Connection Example of MKY35 Basic Functions

Figure 3.11 shows connection example of the MKY35 basic functions. In the example circuit, IO mode 1 is selected. All the expanded functions (except the #MON pin function) described later are unused. The satellite addresses of the MKY35 can be set by DIP-Switch (DIP-SW).

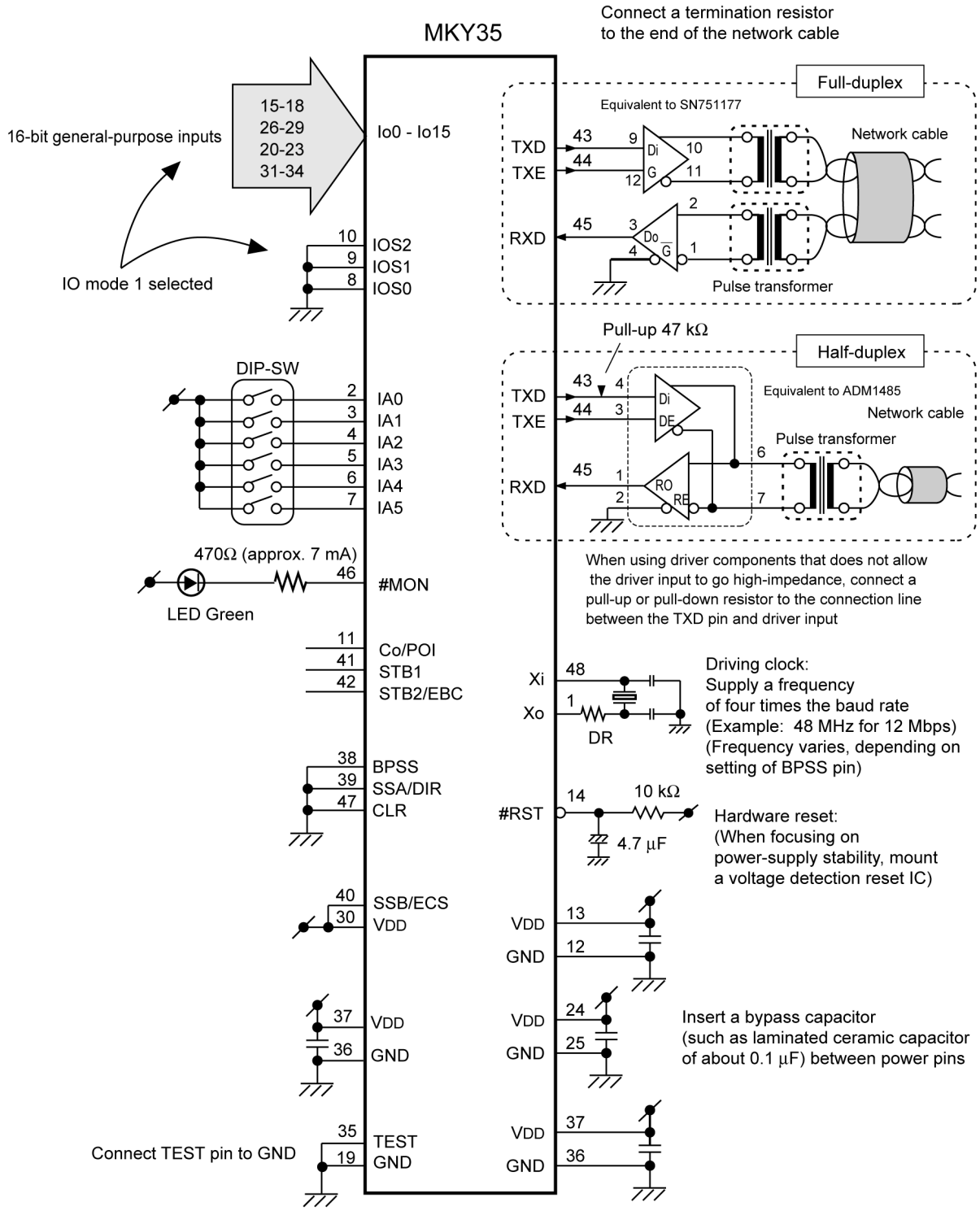

Fig. 3.11 Connection Example of Basic Functions

Chapter 4 Expanded Functions of MKY35

This chapter describes the pin functions and connections required to operate the expanded functions of the MKY35.

Chapter 4 Expanded Functions of MKY35

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4.1 Scan Response Signals and its Applications

This section describes how to use the following two functions among the expanded functions described in ***"1.5.2 Expanded Functions"***:

(1) Has pin that outputs scan response signals
(2) Has CLR pin that sets internal output terminals (Do0 to Do15) Low

4.1.1 Function of #MON Pin

The MKY35 has a #MON pin (pin 46) that outputs scan response signals.
The #MON pin operates as follows by a retriggerable one-shot multivibrator circuit in the MKY35:

(1) The #MON pin goes High when hardware reset becomes activated
(2) After that, when the #MON pin receives command packet (self-addressed CP) transmitted from the center IC to addresses matching SAs set to IA0 to IA5 correctly, it goes Low
(3) After that, when the #MON pin cannot receive self-addressed CP within a given time, it goes High

The "given time" mentioned above varies with the HLS operating state. It ranges from "393216 × driving clock (min.)" to "458752 × driving clock (max.)". Table 4-1 lists the given time for the driving clock.

Table 4-1 Given Time for #MON Pin to Change to High

	BPSS = Low level			BPSS = High level		
Xi Pin frequency	Driving clock	Min. time	Max. time	Driving clock	Min. time	Max. time
48 MHz	48 MHz	8.192 ms	9.557 ms	24 MHz	16.384 ms	19.115 ms
24 MHz	24 MHz	16.384 ms	19.115 ms	12 MHz	32.768 ms	38.229 ms
12 MHz	12 MHz	32.768 ms	38.229 ms	6 MHz	65.536 ms	76.459 ms

Reference In a user system using output signals from the #MON pin as time-up signals for a watchdog timer, set the minimum time as the time-up.

4.1.2 Indication of Scan Response

When the LED that goes on at a Low level is connected to the #MON pin (pin 46), it indicates that the MKY35 has responded to a scanning from the center IC. The #MON pin has a drive capacity of ±8 mA. If the LED can go on even at 8 mA or less, the connection in Figure 4.1 is possible. In this case, the hardware designer of the terminal with the MKY35 needs to determine the current-limiting resistor value according to the LED rating.

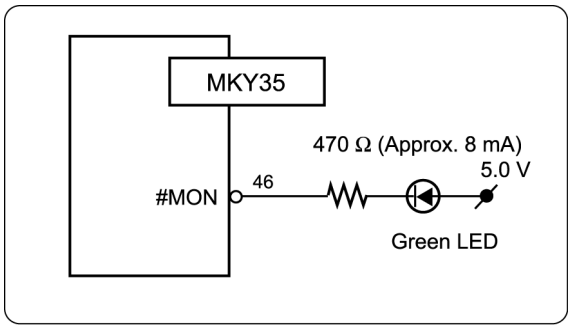

Fig. 4.1 Indication of Scan Response

StepTechnica recommends a green LED indicating stability be connected to the #MON pin. When not used, leave this pin open.

4.1.3 Watchdog Timer

The function of the #MON pin changing from Low to High after the given time has elapsed (time-up) can be used as a watchdog timer for the terminal with the MKY35 embedded.

Generally, the time-up time of a watchdog timer needs to be set longer than the allowable time of multiple scan times. However, the time-up time of the #MON pin may be inappropriate in the following cases:

(1) For the user system where HUBs are inserted into network (One scan time increases according to the inserted number of HUBs.)
(2) When user program operating center IC pauses scanning
(3) When user program operating center IC uses single scan and starts single scan according to inappropriate timing for time-up time of watchdog timer
(4) When user program operating center IC stops scanning intentionally

The user should determine whether the time-up time of the #MON pin is appropriate for the user system.

Reference For details of the scan time, scan pausing, and single scan, refer to ***"User's Manual"*** for the center IC that the MKY35 is connected to.

4.1.4 CLR Pin Function

The MKY35 has a CLR (CLeaR) pin (pin 47) that forcibly sets the internal output terminals (Do0 to Do15) Low. When a High level is input to the CLR pin, all the states of the internal output terminals (Do0 to Do15) go Low. Accordingly, of the 16 Io pins (Io0 to Io15), the Io pins connected to the internal output terminals (Do0 to Do15) by setting the IOS (IO Select) pins are also set Low. In normal operation, design so that a Low level is input to the CLR pin. If a period in which the High-level signal has been input is less than "one clock", the signal is ignored to prevent malfunctions.

The state of the internal output terminals (Do0 to Do15) of the MKY35 is updated each time the command packet (CP) from the center IC transmitted to the addresses matching the SAs set by the IA0 to IA5 pins is received correctly. However, if scanning is stopped for reason such as the disconnection of a network cable or center IC faults, the state of the internal output terminals (Do0 to Do15) is retained continuously.

In a user system in which the state of the internal output terminals (Do0 to Do15) is retained inappropriately when scanning is stopped, the MKY35 can use the CLR pin to forcibly clear the state of the internal output terminals (Do0 to Do15) (Low level). Figure 4.2 shows an example of clearing the state of the internal output terminals (Do0 to Do15) by connecting the signal from the #MON pin as a watchdog timer to the CLR pin.

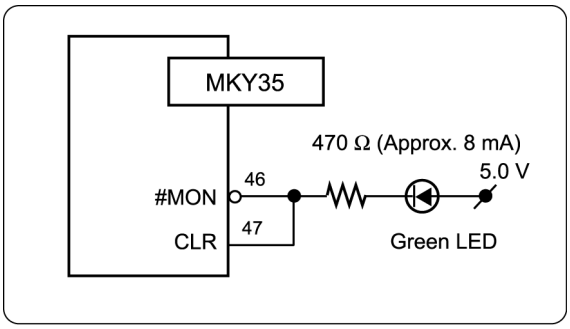

Fig. 4.2 Connection Example between #MON Pin and CLR Pin

Caution Read and understand the description in ***"4.1.3 Watchdog Timer"*** before using this circuit example.

4.2 Setting Strobe Signal and its Application

This section describes how to use the following two functions among the expanded functions described in ***"1.5.2 Expanded Functions"***:

(3) Has strobe output pins that indicate when to update internal output terminals (Do0 to Do15) and a timing to receive internal input terminals (Di0 to Di15)
The user can design peripheral circuit based on each update timing

(4) Can set handshake to ensure link with center IC

4.2.1 STB1 Pin Function

Each time the MKY35 receives the command packet (CP) matching the SA from the center IC correctly, it outputs data in the CP to the internal output terminals (Do0 to Do15) of the MKY35. The state of the internal output terminals (Do0 to Do15) is updated at "1/4" to "1/2" timing of the pulse-like strobe signal from the STB1 (STroBe-1) pin (pin 41) (Fig. 4.3). Consequently, the state of the Io pins set to "output" also changes around the same time. The function of this STB1 pin can be used to notify a circuit connected to the Io pins set to "output" that the output state is updated.

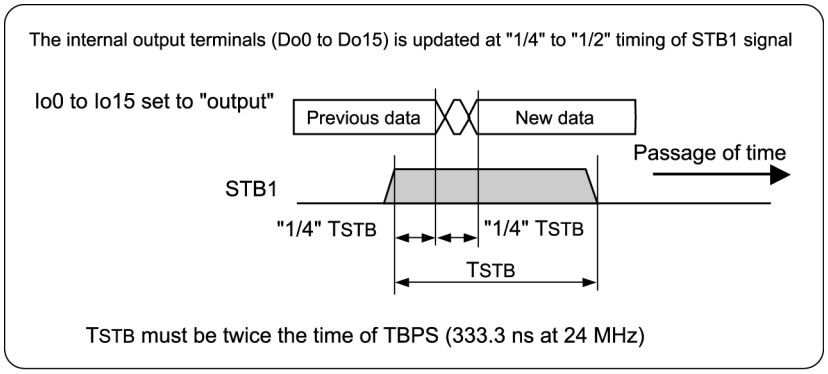

Fig. 4.3 Update Timing of Internal Output Terminals (Do0 to Do15)

Reference The pulse-like strobe signal output from the STB1 pin is unaffected by the command value of the center IC. The strobe signal is also output from the STB1 pin if the state of the internal output terminals after updating is identical to that before updating.

4.2.2 Time to Sample State of Io Pin (STB2 Pin)

If the command in the CP issued from the center IC is "0" when the response packet (RP) is returned in response to the command packet (CP) matching the SA, the MKY35 samples the internal input terminals (Di0 to Di15). The MKY35 outputs a pulse-like strobe signal from the STB2 (STroBe-2) pin (pin 42) to indicate the time to sample the state of the internal input terminals (Di0 to Do15). The state of the internal input terminals (Di0 to Di15) is sampled at the beginning of the strobe signal. Since the bits of the internal input terminals that are not connected to the Io pins are connected to GND, the bit value of data to be sent to the center IC is "0".

Reference When the SSB (Strobe Select-B) pin described in ***"4.2.4 Enabling/Disabling Handshake (SSB Pin)"*** is Low, no strobe signal may be output from the STB2 pin when the MKY35 returns the RP.

4.2.3 Setting Strobe Signal Timing (SSA Pin)

The following two requests occur in the user system using the HLS:

(1) To update output state of Io pins set to “output” after sampling input state of Io pins set to “input”.
(2) To sample input state of Io pins set to “input” after updating output state of Io pins set to “output”.

In the MKY35, the user can select the timing of strobe signals output from the STB1 pin and STB2 pin by setting the SSA (Strobe Select-A) pin (pin 39). This will enable to meet the two requests. The MKY35 performs the operation in (1) above when the SSA pin is set Low, and the operation in (2) above when the SSA pin is set High (Fig. 4.4).

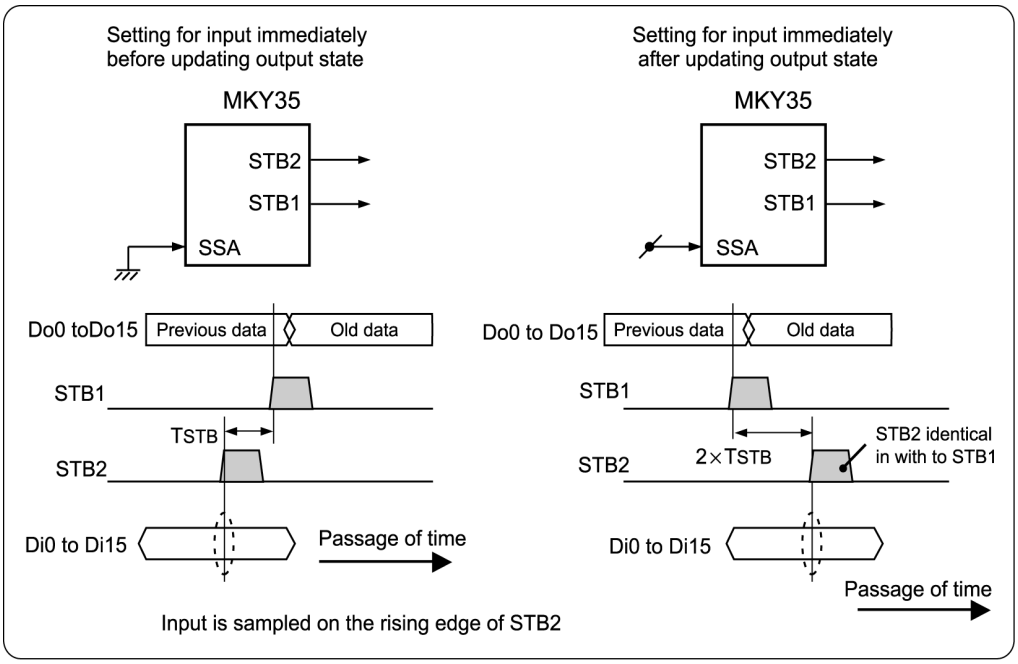

Fig. 4.4 SSA Pin Setting and Update Timing

4.2.4 Enabling/Disabling Handshake (SSB Pin)

Handshaking with the center IC can be enabled or disabled by setting the SSB (Strobe Sdect-B) pin (pin 40). When the SSB pin is Low, handshaking with the center IC is enabled.

When the MKY35 inputs the self-addressed command packet (CP) from the center IC, it recognizes whether the center IC has received correctly the response packet (RP) returned to the center IC at the last scan. In a case where handshaking is enabled, the MKY35 outputs a strobe signal from the STB2 pin to sample the internal input terminals (Di0 to Di15) only when the center IC has input the previously returned RP correctly, and the sampled state of the internal input terminals (Di0 to Di15) is embedded in the RP.

If the center IC has not input the previously returned RP correctly, the MKY35 neither outputs a strobe signal to the STB2 pin nor samples the state of the internal input terminals (Di0 to Di15). In this case, the previously sampled state of the internal input terminals (Di0 to Di15) is embedded in the RP again. Figure 4.5 shows the timing of generating the STB2 strobe signal in the MKY35 with five satellites and "SA = 2" in half-duplex mode.

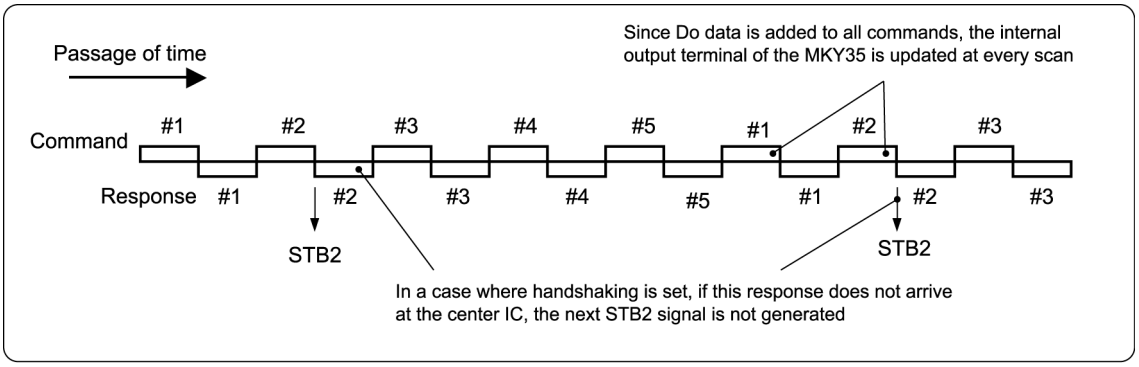

Fig. 4.5 Timing of STB2 Strobe Signal Generation

Reference In a user system in which real-timeness is essential when a sensor is connected to the Io pins set to "input", and so on, disable handshaking.

4.2.4.1 Example of Handshaking Effectiveness

This section describes an example of the effectiveness of handshaking with the center IC.

Some user systems may want to send character string data to the center IC in synchrony with the strobe signal output from the STB2 pin. For example, when transferring character string data consisting of the 5 characters **"ABCDE"** to the Io pin (Di) of the MKY35 set to "input" one-by-one at each output of the STB2 strobe signal (Fig. 4.6A), a character may be omitted in the character string data obtained by the center IC when handshaking with the center IC is disabled. For example, if there is interference including external noise in the network during sending the letter **"C"** and the RP is discarded at the center IC, the STB2 strobe signal is output at the next scan. Consequently, the center IC receives the character string data **"ABDE"** (**"C"** omitted) (Fig. 4.6B).

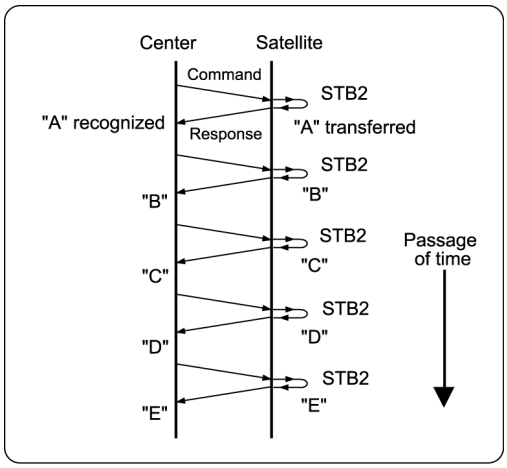

Fig. 4.6A Operation with No Failure

In contrast, when handshaking is enabled, the STB2 strobe signal is not output at the next scan even when the RP is discarded at the center IC and character will not be omitted (Fig. 4.6C).

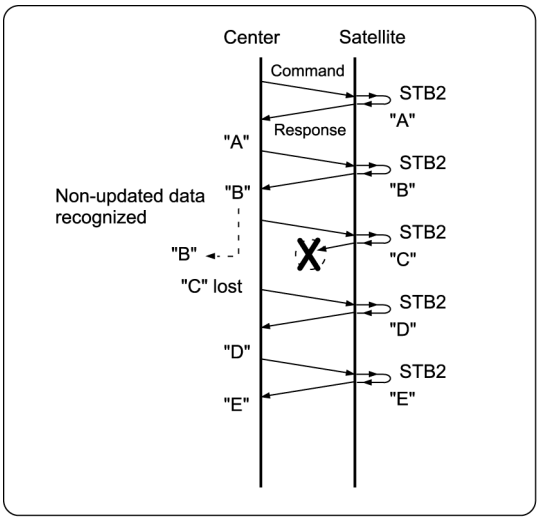

Fig. 4.6B Handshaking Disabled

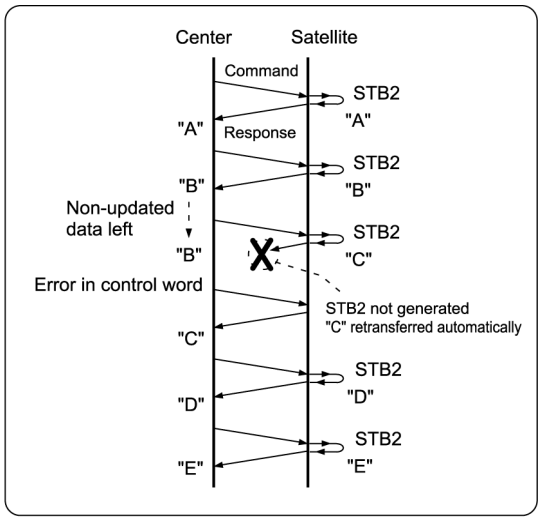

Fig. 4.6C Handshaking Enabled

4.2.4.2 Cautions for Sending Character String Data

This section describes the cautions for sending character string data when handshaking is enabled with the SSB pin set Low.

As described previously, enabling handshaking ensures that character string data is sent (without omitting character) to memory in the center IC. In this case, the user system program of the center IC must obtain character string data from memory in synchronization with scan timing. For the example in Figure 4.6C, note the following:

(1) If character string data is simply obtained from memory in synchronization with the scan timing, the character string data including duplicated characters like **"ABBCDE"** may be read (because the third character cannot reach at the third scan).
(2) At the third scan, the corresponding satellite IC causes an error (that can be recognized by a nonresponding flag bit in the control word in the center IC).
(3) If the above error occurs, ideally it should be handled by the algorithm that does not read data. However, since scanning is very fast and such handling must be set for each satellite IC, program execution speed may not follow scan speed.

Based on the above cautions, a method for easily creating the program algorithm for the center IC is shown below.

When all the 16 Io pins (Io0 to Io15) are set to "input", if eight pins are used to input a character code (8-bit information), eight pins are left. When a "character counter" is used for these eight Io pins, the program algorithm for the center IC can be created easily. Figure 4.7 shows a example of using the high-order one byte (8 bits) of data as a character counter.

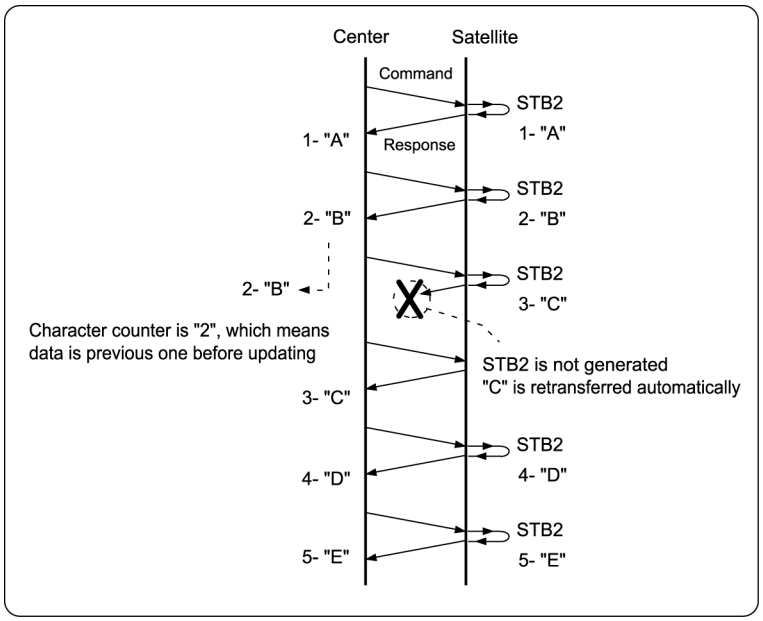

Fig. 4.7 Sending with Character Counter Used

4.2.4.3 Caution for Using Handshaking (1)

In the HLS, the handshaking function is intended to send data sampled by the satellite IC to the center IC without loss. This will cause a difference in data arrival at the center IC between when an error occurs in the response packet and when an error occurs in the command packet.
An example of sending character string data is shown. If an error occurs in the response packet (Figs. 4.6C and 4.7), the letter **"C"** does not arrive at link failure and does arrive at the next normal scan. In contrast, if an error occurs in the command packet (Fig. 4.8), the letter **"B"** arrives at the center IC twice at the scan before or after link failure.

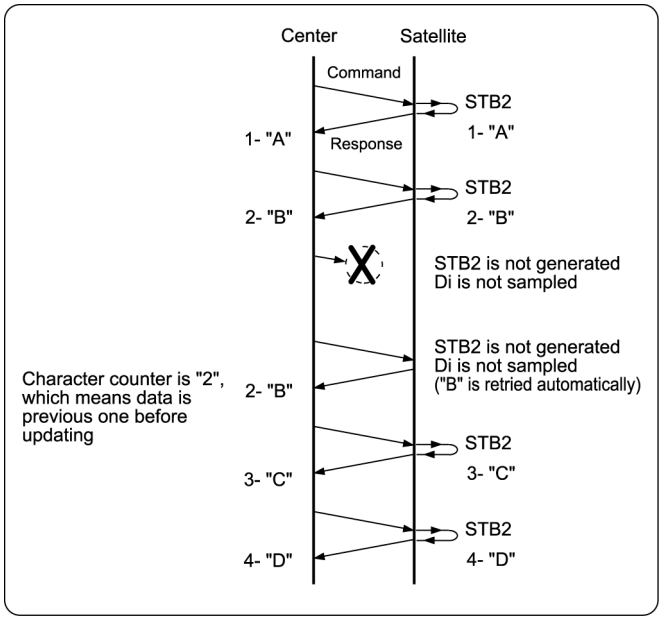

Fig. 4.8 Operation at CP Failure

As shown in this example, in both cases, the data sampled by the satellite IC is sent to the center IC without loss. However, based on the difference in data arrival at the center IC, the user system program must handle data in the center IC (memory). Placing a character counter of at least two or more bits as described in ***"4.2.4.2 Cautions for Sending Character String Data"*** near the MKY35 can help the user system program to deal with this problem.

4.2.4.4 Caution for Using Handshaking (2)

When the SSB pin (pin 40) is set to enable the handshaking, and when the user system executes commands other than "0" or "8" (basic function specified) for the MKY35, no strobe signal is output from the STB2 pin.

If the MKY35 is set in the PWM mode described later, the SSA input pin forcibly retains Low internally (STB2 signal is generated before STB1 signal) and the SSB input pin forcibly retains High internally (handshaking disabled).

4.3 PWM Modes

This section describes two types of PWM (Pulse Width Modulation) modes described in (5) in ***"1.5.2 Expanded Functions"***.

4.3.1 PWM Mode 1

The MKY35 is set in PWM mode 1 when the IOS2 pin set High, the IOS1 pin High, and the IOS0 pin Low. In PWM mode 1, a PWM circuit is inserted between the internal output terminals (Do0 to Do7) and the Io pins (Io12 to Io15) (Fig. 4.9). Pins 11 and 42, which are the Co output pin and STB2 output pin in the IO mode, function as the input-only pins (POI: Pwm On Invert, and EBC: External Base Clock) of the PWM circuit; pins 39 and 40, which are the SSA input pin and SSB input pin in the IO mode, function as the input-only pins (DIR: DIRection, and ECS: External Clock Select) of the PWM circuit. In PWM mode 1, the internal output terminals (Do8 to Do11) and internal input terminals (Di0 to Di7) can be used just as those in the IO mode.

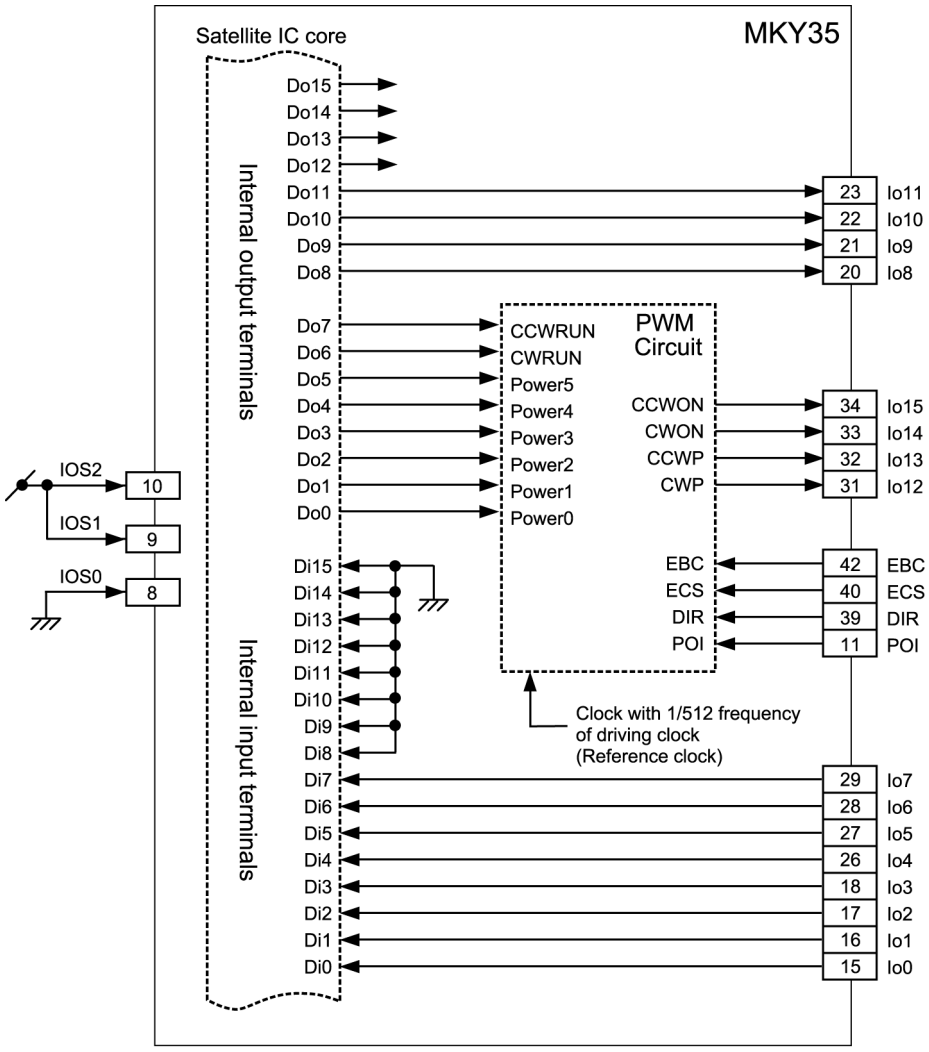

Fig. 4.9 PWM Mode 1

Caution If the MKY35 is set in the PWM mode, the SSA input pin forcibly retains Low internally (STB2 signal is generated before STB1 signal) and the SSB input pin forcibly retains High internally (handshaking disabled). The Co output pin and STB2 output pin cannot be used.

4.3.2 PWM Circuit

The PWM (Pulse Width Modulation) circuit of the MKY35 is a circuit that generates a clock that can change the duty ratio (Fig. 4.10). The duty ratio are proportional to the Power values (00H to 3FH) set to Power 0 to Power 5 (internal output terminals Do0 to Do5). The clock period is determined by the "reference clock" supplied to the PWM circuit. The pulse signal generated by the PWM circuit is called a "PWM signal". However, the "PWM signal" serves as a High-level status instead of as a clock only when the Power value is set to 3FH.

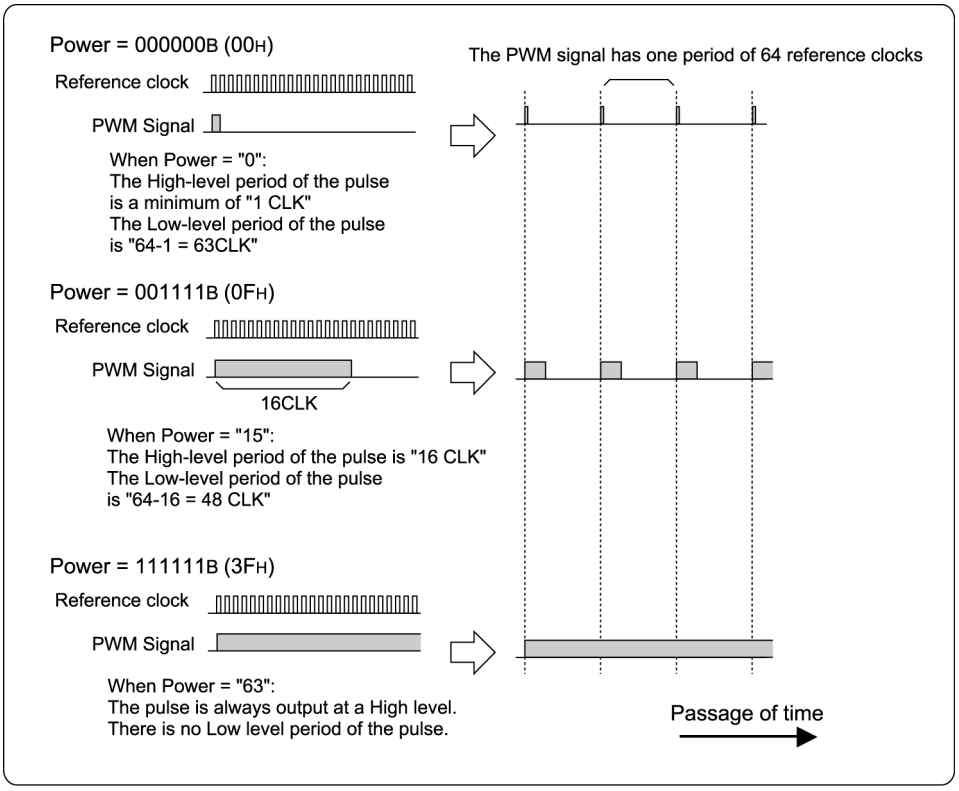

Fig. 4.10 PWM Signal

The formula for the duty ratio of the PWM signal to the Power value is shown below:

[Duty ratio] (Power value + 1) ÷ 64

Example: Power value = 0 (00H). . . . . Duty ratio = (0 + 1) ÷ 64 ≠ 1.6%
Example: Power value = 15 (0FH). . . . Duty ratio = (15 + 1) ÷ 64 = 25.0%
Example: Power value = 32 (20H) . . Duty ratio = (32 + 1) ÷ 64 ≠ 51.5%
Example: Power value = 63 (3FH). . . . Duty ratio = (63 + 1) ÷ 64 = 100%

4.3.2.1 Basic Operation of PWM Circuit

The CWP (Clock Wise Pulse) and CCWP (Counter-Clock Wise Pulse) output pins of the PWM circuit output PWM signals.
The CWON (Clock Wise ON) and CCWON (Counter-Clock Wise ON) output pins output PWM enable signals.
The DIR (DIRection), POI (Pwm On Invert), CWRUN (Clock Wise RUN), and CCWRUN (Counter-Clock Wise RUN) input pins control the output of PWM signals.
The ECS (External Clock Select) input pin selects the reference clock for the PWM signal.
The EBC (External Base Clock) input pin supplies the reference clock for the PWM signal.
When the input state of the DIR, POI, ECS, and EBC pins are set Low, the PWM circuit executes the following basic operation:

(1) When the CWRUN (internal output terminal Do6) is set High, the CWON (Io14 pin) is set High and the PWM signal is output from the CWP (Io12 pin).
(2) When the CCWRUN (internal output terminal Do7) is set High, the CCWON (Io15 pin) is set High and the PWM signal is output from the CCWP (Io13 pin).
(3) When both the CWRUN and CCWRUN are set High, no pulse is output from the CWP and CCWP, and the CWON, CCWON, CWP, and CCWP are set Low.
(4) A clock with a frequency of 1/512 of the MKY35 driving clock is used as a reference clock to generate a PWM signal. Table 4-2 shows the driving clocks, reference clocks of PWM signals, and clock periods.

Table 4-2 Driving Clocks, Reference Clocks of PWM Signals, and Clock Periods

	BPSS = Low level			BPSS = High level		
Xi Pin frequency	Driving clock	Reference clock of PWM circuit	PWM Signal period	Driving clock	Reference clock of PWM circuit	PWM Signal period
48 MHz	48 MHz	93.7500 kHz	≈ 1.465 kHz	24 MHz	46.8750 kHz	≈ 732.42 Hz
24 MHz	24 MHz	46.8750 kHz	≈ 732.42 Hz	12 MHz	23.4375 kHz	≈ 366.21 Hz
12 MHz	12 MHz	23.4375 kHz	≈ 366.21 Hz	6 MHz	11.71875 kHz	≈ 183.11 Hz

4.3.2.2 Functions of ECS and EBC Pins

The ECS (External Clock Select) pin of the PWM circuit selects and sets the reference clock to generate a PWM signal as follows:

(1) When the ECS pin is set Low, a clock with a frequency of 1/512 of the driving clock of the MKY35 is used as a reference clock for a PWM signal (Table 4-2).
(2) When the ECS pin is set High, the clock supplied to the EBC (External Base Clock) pin is used as a reference clock for a PWM signal. The maximum frequency that can be input to the EBC pin is 50 MHz, and the minimum High-level and Low-level widths are 10 ns.

In (1) above, keep the EBC pin High or Low so that it does not enter the open state.

4.3.2.3 Function of DIR Pin

The DIR (DIRection) pin of the PWM circuit replaces the direction concept indicated by CW (Clock Wise) and CCW (Counter-Clock Wise).
When the DIR pin is High, operations (1) and (2) described in ***"4.3.2.1 Basic Operation of PWM Circuit"*** change as follows:
(1) When the CWRUN (internal output terminal Do6) is set High, the CCWON (Io15 pin) is set High and the PWM signal is output from the CCWP (Io13 pin).
(2) When the CCWRUN (internal output terminal Do7) is set High, the CWON (Io14 pin) is set High and the PWM signal is output from the CWP (Io12 pin).

4.3.2.4 Function of POI Pin

The POI (Pwm On Invert) pin of the PWM circuit reverses the logic of the CWON and CCWON outputs to output a PWM enable signal.
When the POI pin is Low, the CWON and CCWON outputs are set High to output a PWM enable signal (refer to (1) and (2) described in ***"4.3.2.1 Basic Operation of PWM Circuit"***).
When the POI pin is High, the CWON and CCWON outputs are set Low to output a PWM enable signal (Fig. 4.11). In addition, when the POI pin is High, (3) described in ***"4.3.2.1 Basic Operation of PWM Circuit"*** is changed as follows:

When both the CWRUN and CCWRUN are set High, no pulse is output from the CWP and CCWP, and the CWON and CCWON are set High and the CWP and CCWP are set Low.

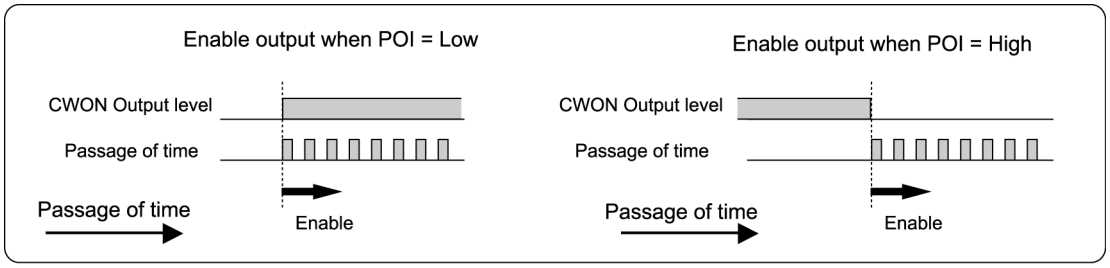

Fig. 4.11 Reverse of Logic of Enable Signal

Caution When not reversing the enable signal using the POI pin, be sure to keep the POI pin Low so that it does not enter the open state.

4.3.2.5 Cautions for Using PWM Function

This section describes the cautions for using the PWM function.

(1) The PWM circuit recognizes the Power values, CWRUN, and CCWRUN every 64 clock periods of the reference clock for a PWM signal. Consequently and regardless of the operating conditions of the PWM circuit, hazards or abnormal short pulse does not occur on output signals from the PWM circuit even if the Power values, CWRUN, and CCWRUN are changed.

(2) The level transition of DIR (DIRection) and POI (Pwm On Invert) inputs is reflected immediately in the CWP, CCWP, CWON, and CCWON outputs. Therefore, StepTechnica advises the user not to change DIR and POI input levels when the PWM function is activated. If the user wants to change the DIR and POI input levels during operation of the PWM function, change them carefully to prevent hazards on abnormal pulse from occurring on the output signals of the PWM circuit).

(3) When designing a system in which switching type power controller (power MOSFET and TRIAC, etc.) are driven by CWP, CCWP, CWON, and CCWON output signals, refer to the section ***"5.2 AC Characteristics"*** and design the system to prevent any trouble.

4.3.2.6 Application Example of PWM Circuit Operation (1)

Figure 4.12 shows an example of control brightness of electric bulb using the PWM circuit.

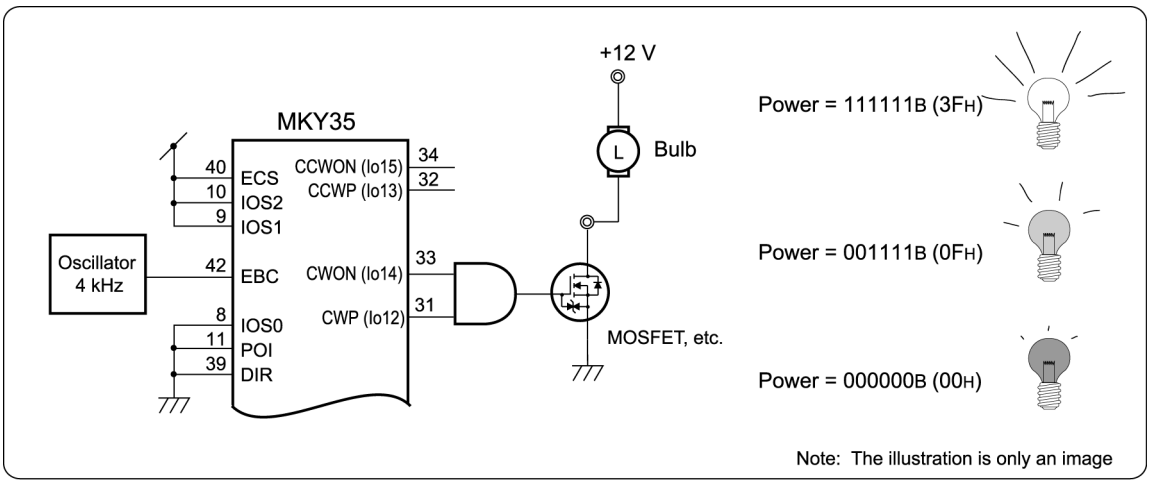

Fig. 4.12 Example of Controlling Bulb Using PWM Function

In this example, the ECS (External Clock Select) input keeps High to supply a 4-kHz clock to the EBC (External Base Clock) input. The PWM signal output from the CWP pin has a pulse period of 16 ms (62.5 Hz), which is close to the commercial power frequency of 60 Hz, resulting in imperceptible flickering even though controlled. The CCWON (Counter-Clock Wise ON) output and CCWP (Counter-Clock Wise Pulse) output are unused and left open.

If a terminal configured as shown in Figure 4.12 is connected to the HLS network, the user system can remotely control the bulb brightness by writing memory (data in the Do area) in the center IC.
For example, the user system can control the bulb brightness by writing a brightness value to the bits corresponding to the Power 0 to Power 5 (internal output terminals Do0 to Do5).
For example, the user system can control the bulb on-off operation by writing “1 (light ON)” or “0 (light OFF)” to the bit corresponding to the CWRUN pin (internal output terminal Do6).

Caution Figure 4.12 shows the concept for controlling a bulb brightness but the operation is not guaranteed. Select the components and reference clocks (including frequencies) according to the system.

4.3.2.7 Application Example of PWM Circuit Operation (2)

Figure 4.13 shows an example of controlling the rotation direction and rotational speed of a DC motor using the PWM circuit.

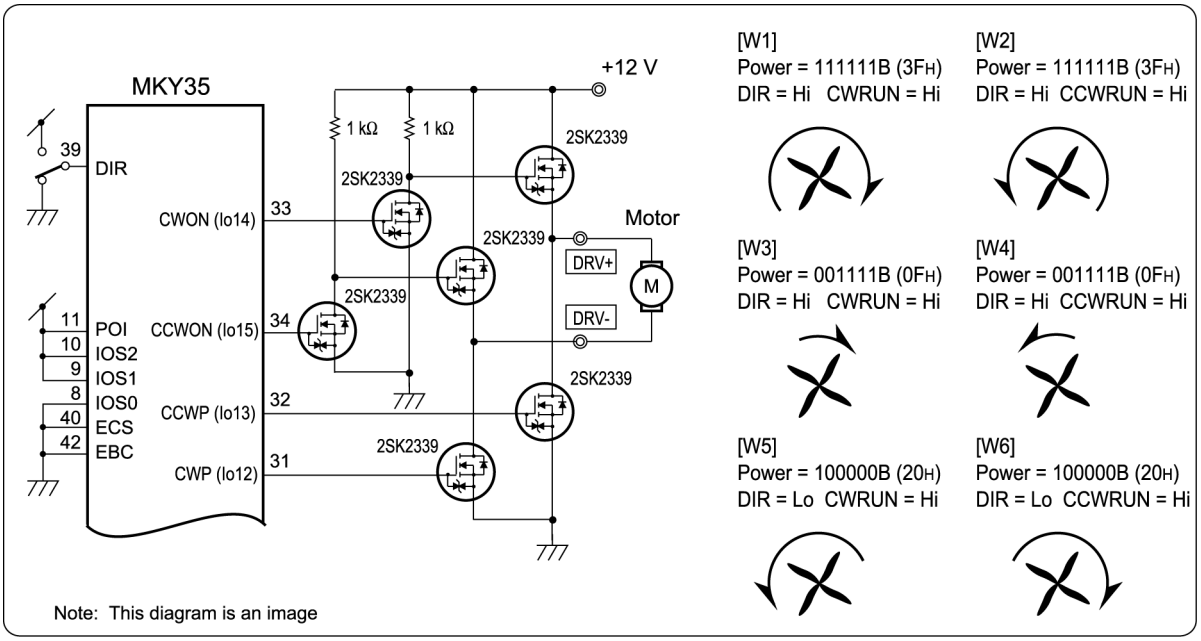

Fig. 4.13 Example of Motor Control Using PWM Function

In this example, the ECS (External Clock Select) and the EBC (External Base Clock) inputs keep Low and use an internal reference clock.
If a terminal with the configuration as shown in Figure 4.13 is connected to the HLS network, the user system can remotely control the rotation direction and rotational speed of a DC motor by writing to memory (data in the Do area) in the center IC.

In Figure 4.13, [W1] shows the fan rotates clockwise when "1" is written to the bit corresponding to the CWRUN (internal output terminal Do6), and values indicating the maximum rotational speed of the motor is written to the bits corresponding to the Power (internal output terminals Do0 to Do5).
[W2] shows the fan rotates counter-clockwise when "1" is written to the bit corresponding to the internal output terminal Do7 (CCWRUN).
[W3] shows the fan rotates clockwise at low speed, and [W4] shows the fan rotates counter-clockwise at low speed.
[W5] and [W6] show the fan rotates at medium speed in a direction opposite to CWRUN and CCWRUN when the input state of the DIR pin changes from Low to High.

When the rotation of the motor axis is transmitted using gears as shown in examples [W5] and [W6], the rotation direction may vary between the actual motion and the rotation direction as control data. In this case, the actual rotation direction and rotation direction as control data can be the same by changing the level of the DIR pin.

Caution Figure 4.13 shows a concept for drive controlling the DC motor but the operation is not guaranteed. Select the components and reference clocks (including frequencies) according to the system.

4.3.3 PWM Mode 2

The MKY35 is set in PWM mode 2 when the IOS2 pin is set to High, the IOS1 pin to High, and the IOS0 pin to High. In PWM mode 2, just as in PWM mode 1, a PWM circuit is inserted between the internal output terminals (Do0 to Do7) and the Io pins (Io12 to Io15). Pins 11 and 42, which are the Co output pin and STB2 output pin in the IO mode, function as input-only pins (POI: Pwm On Invert, and EBC: External Base Clock) of the PWM circuit, and pins 39 and 40, which are the SSA input pin and SSB input pin in the IO mode, function as the input-only pins (DIR: DIRection, and ECS: External Clock Select) of the PWM circuit. In PWM mode 2, a universal counter is also inserted between the internal input terminals (Di0 to Di11) and the Io pins (Io4 to Io7) (Fig. 4.14), and the internal output terminals (Do8 to Do11) can be used just as in the IO mode. The Io pins (Io0 to Io3) are connected to the internal input terminals (Di12 to Di15). The operation of the PWM circuit in PWM mode 2 is the same as that in PWM mode 1. For details, refer to ***"4.3.2 PWM Circuit"***.

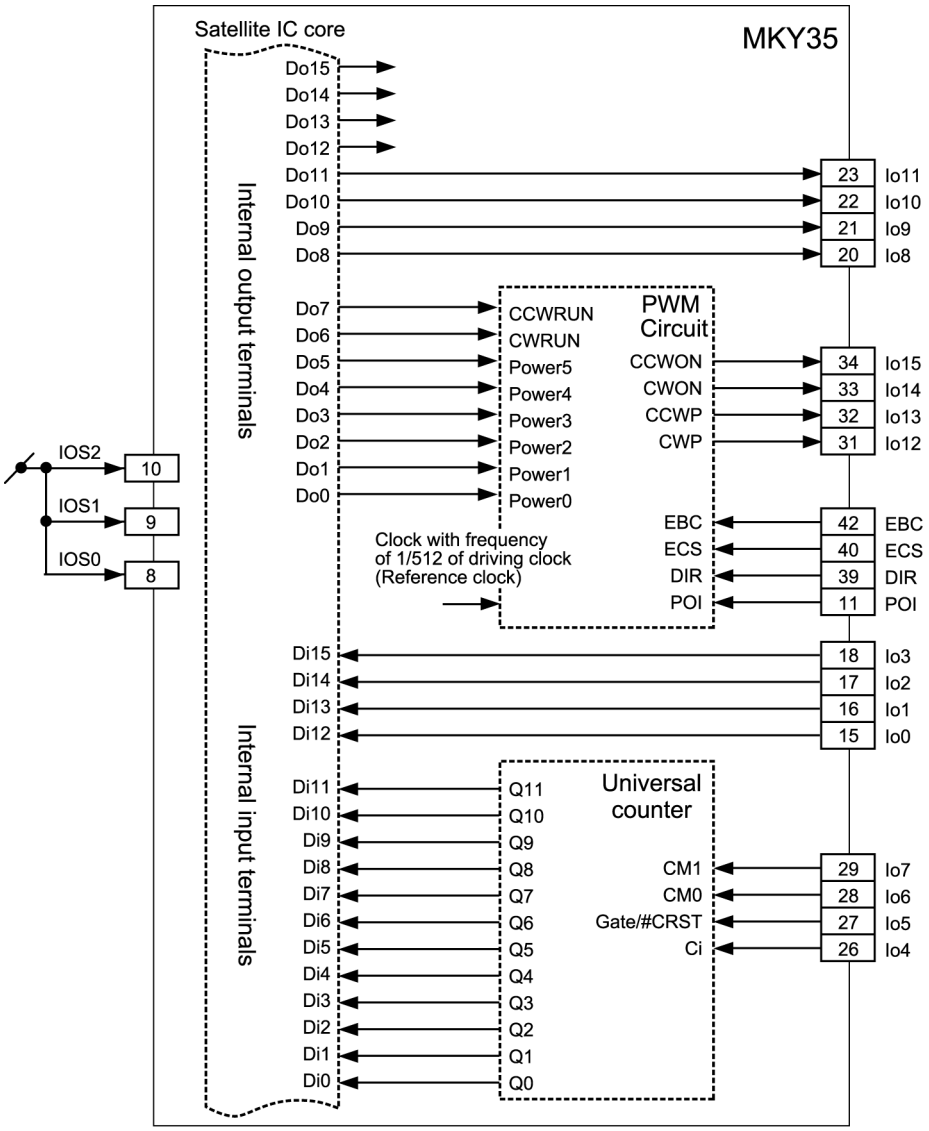

Fig. 4.14 PWM Mode 2

Caution If the MKY35 is set in the PWM mode, the SSA input pin forcibly retains Low internally (STB2 signal is generated before STB1 signal) and the SSB input pin forcibly retains High internally (handshaking disabled). The Co output and STB2 output cannot be used.

4.3.4 Universal Counter

The universal counter inserted between the internal input terminals (Di0 to Di11) and the Io pins (Io4 to Io7) in PWM mode 2 has a 12-bit binary up-counter. The 12-bit count values are connected to the internal input terminals (Di0 to Di11). When a terminal in PWM mode 2 is connected to the HLS network, the user system can remotely reference the count values by reading memory (data in the Di area) in the center IC.
The operating specifications for the universal counter are as follows:

(1) The Low to High transition of a signal input to the Ci pin connected to the Io4 pin is counted from 000H to FFFH.
(2) When the Low to High transition is input to the Ci pin following FFFH, counting starts with 000H.
(3) The High-level and Low-level widths of a signal input to the Ci pin should be longer than "1.5 × TBPS". For example, if the baud rate is 12 Mbps, the High level and Low level must be 125 ns or more.
(4) When the MKY35 hardware reset is activated, the count value is reset to 000H.

The universal counter has four count modes shown in Table 4-3. The count mode varies depending on the combination of levels of the CM0 pin connected to the Io6 pin and the CM1 pin connected to the Io7 pin.

Table 4-3 Count Modes

Io7	Io6	Counter mode	Function of Io5 pin
Lo	Lo	Free count mode	#CRST
Lo	Hi	Internal gate 1 mode	Unused input. Should be kept High or Low.
Hi	Lo	Internal gate 2 mode	Unused input. Should be kept High or Low.
Hi	Hi	External gate mode	Gate

4.3.4.1 Free Count Mode

When the CM0 (Io6) pin and CM1 (Io7) pin are Low, the universal counter is in free count mode. In this mode, the Low to High transition of a signal input to the Ci (Io4) pin is counted while the #CRST (Io5) pin of the universal counter is High. When the #CRST pin goes Low, the 12-bit binary up-counter in the universal counter is reset to 000H. The Low to High transition of a signal input to the Ci pin (Io4) is not counted while the #CRST pin is Low. Figure 4.15 shows an internal equivalent circuit in free count mode.

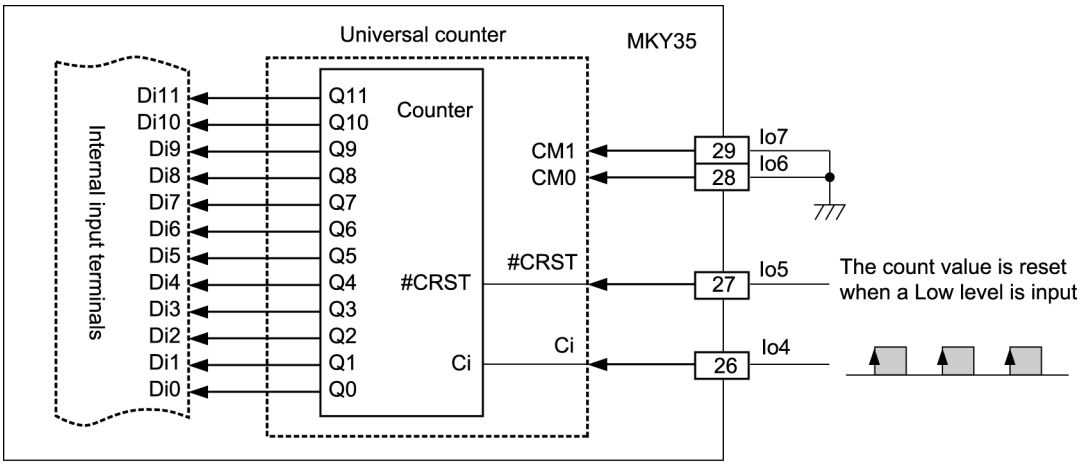

Fig. 4.15 Equivalent Circuit in Free Count Mode

4.3.4.2 Internal Gate 1 Mode

When the CM0 (Io6) pin is High and the CM1 (Io7) is Low, the universal counter is in internal gate 1 mode. In this mode, a clock with a frequency of 1/4,194,304 (2^{22}) of the MKY35 driving clock is generated as a gate signal. Figure 4.16 shows an internal equivalent circuit in the internal gate 1 mode.

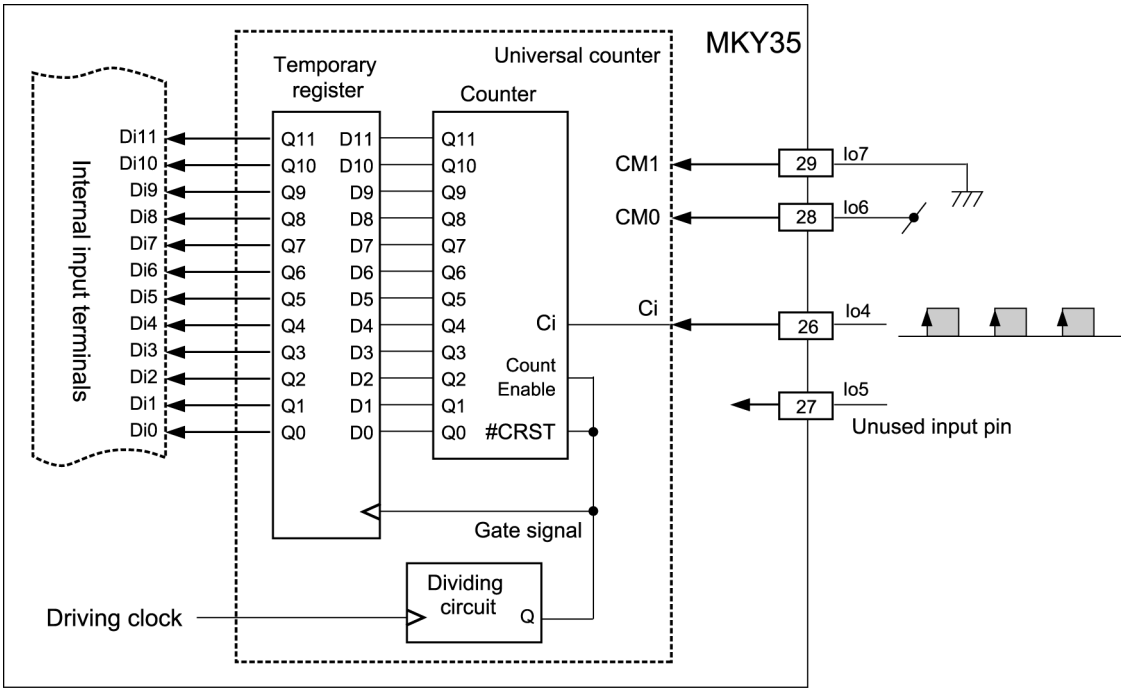

Fig. 4.16 Equivalent Circuit in Internal Gate 1 Mode

The output pins of the temporary register are connected to the internal input terminals (Di0 to Di11).
When the MKY35 hardware reset is activated, the temporary register is reset to 000H.
The counter unit operates for the gate signal as follows (Fig. 4.17):

(1) The Low to High transition of a signal input to the Ci pin connected to the Io4 pin is counted while the gate signal is High.
(2) When the gate signal transits to Low, the count value is held in the temporary register.
(3) When the gate signal transits to High, the counter is reset to 000H and gets ready for the next count of input to the Ci pin.

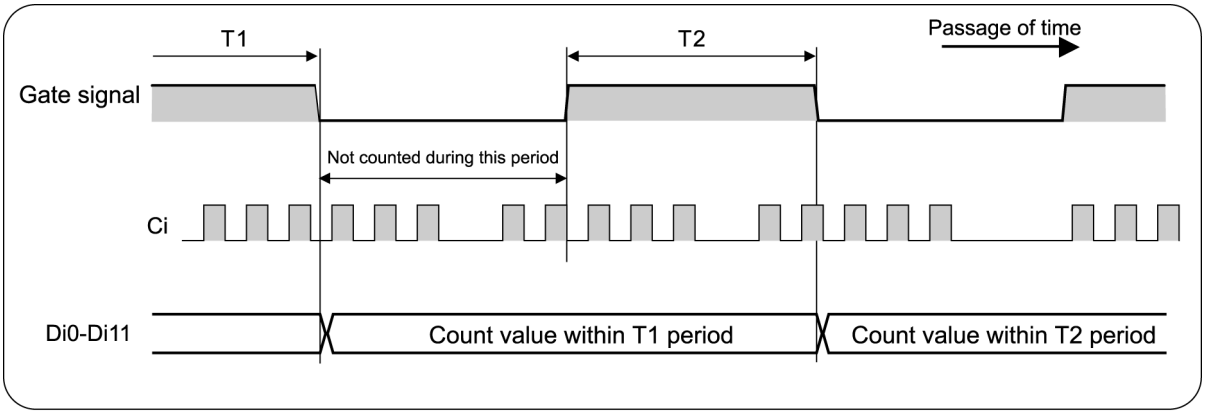

Fig. 4.17 Operation of Gate Counter

Table 4-4 lists the gate times corresponding to the driving clock frequencies.
When using the internal gate 1 mode, the Io5 pin serves as an unused input pin. Keep it High or Low.

Table 4-4 Gate Times in Internal Gate 1 Mode

	BPSS = Low level			BPSS = High level		
Xi Pin frequency	Driving clock	Gate signal	Gate time	Driving clock	Gate signal	Gate time
48 MHz	48 MHz	≈ 11.444 Hz	≈ 43.69 ms	24 MHz	≈ 5.722 Hz	≈ 87.38 ms
24 MHz	24 MHz	≈ 5.722 Hz	≈ 87.38 ms	12 MHz	≈ 2.861 Hz	≈ 174.76 ms
12 MHz	12 MHz	≈ 2.861 Hz	≈ 174.76 ms	6 MHz	≈ 1.430 Hz	≈ 349.53 ms

4.3.4.3 Internal Gate 2 Mode

When the CM0 (Io6) pin is Low and the CM1 (Io7) is High, the universal counter is in internal gate 2 mode. In this mode, a clock with a frequency of 1/67,108,864 (2^{26}) of the MKY35 driving clock is generated as a gate signal.

The difference between the internal gate 2 mode and internal gate 1 mode is a period and High-level width of the gate signal, and the equivalent circuit and counter operation are identical. Table 4-5 lists the gate times corresponding to the drive-clock frequencies. When using the internal gate 2 mode, the Io5 pin serves as an unused input pin. Keep it High or Low.

Table 4-5 Gate Times in Internal Gate 2 Mode

	BPSS = Low level			BPSS = High level		
Xi Pin frequency	Driving clock	Gate signal	Gate time	Driving clock	Gate signal	Gate time
48 MHz	48 MHz	≈ 0.7153 Hz	≈ 0.699 s	24 MHz	≈ 0.3576 Hz	≈ 1.398 s
24 MHz	24 MHz	≈ 0.3576 Hz	≈ 1.398 s	12 MHz	≈ 0.1788 Hz	≈ 2.796 s
12 MHz	12 MHz	≈ 0.1788 Hz	≈ 2.796 s	6 MHz	≈ 0.0894 Hz	≈ 5.592 s

4.3.4.4 External Gate Mode

When the CM0 (Io6) pin and CM1 (Io7) pin are High, the universal counter is in external gate mode. In this mode, the signal supplied to the Gate (Io5) pin from outside the MKY35 is used as the gate signal described in ***"4.3.4.2 Internal Gate 1 Mode"***. Figure 4.18 shows an equivalent circuit in the external gate mode. Prepare the gate signal supplied to the Gate (Io5) pin according to the user system.

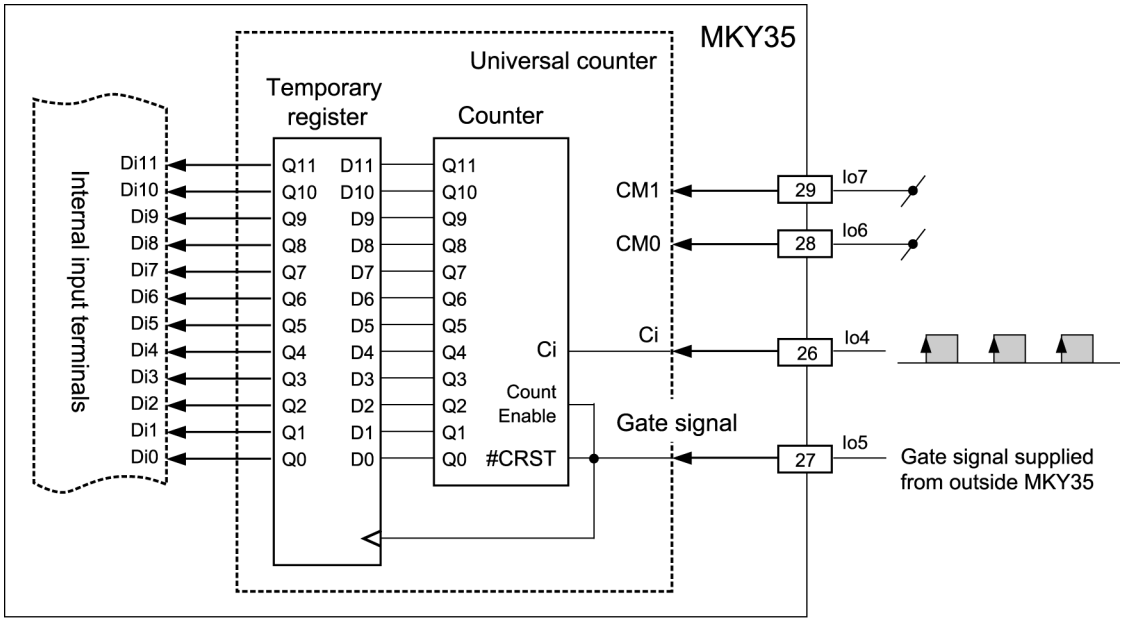

Fig. 4.18 Equivalent Circuit in External Gate Mode

4.3.4.5 Application Example of Gate Counter

Figure 4.19 shows an example of application using the gate counter.

This shows a circuit with rotational speed detection of the DC motor, as well as rotation control of the motor using the PWM circuit described in section ***"4.3.2.7 Application Example of PWM Circuit Operation (2)"***. In this example, a transmission optical sensor detects the rotational state of the fan driven by motor rotation, and the output of the optical sensor is input to the Ci (Io4) pin of the universal counter. The count mode is the internal gate 2 mode.

If a baud rate of 6 Mbps is set for the MKY35, the gate time of the counter is about 1.398 s. If the optical sensor detects four fan blades and the count value within gate time is 188 (0BCH), the calculation (188 ÷ 4) ÷ 1.398 s × 60 s shows that the fan rotates at 2017 rpm.

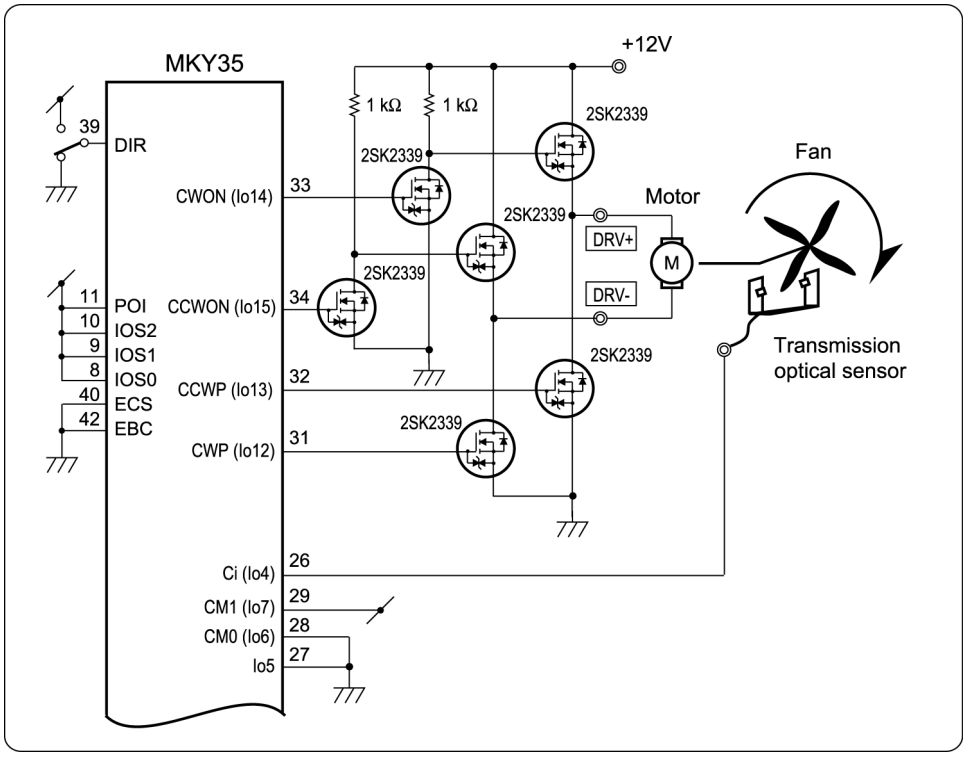

Fig. 4.19 Example of Feedback Control of Rotational Speed

If a terminal with the configuration as shown in Figure 4.19 is connected to the HLS network, the user system can easily:

(1) Control remotely the rotation direction and rotational speed of the DC motor by writing to memory (data in the Do area) in the center IC.

(2) Recognize remotely the rotational speed of the fan by reading from memory (data in the Di area) in the center IC.

(3) Perform feedback control of the fan rotational speed using (1) and (2) above.

Caution Figure 4.19 shows a concept for controlling of the DC motor with feedback but the motor operation is not guaranteed. Select the components and reference clocks (including frequencies) according to the user system.

4.3.4.6 Application of Gate Counter

In the internal gate 1, internal gate 2, or external gate modes, the gate counter counts signal transitions within a given time. This operation is the same as that of a frequency counter. Therefore, a frequency counter can be configured by selecting a proper gate signal or performing arithmetic operations on the obtained counts in order to match the gate signal.

For example, in the external gate mode, if the count value (QV) is 1500 (5 DCH) when a 1-kHz clock (GF) is input to the Gate (Io5) pin, the frequency (F) of the signal input to the Ci (Io4) pin is determined as a digital value within a ±1-digit accuracy as follows:

$$2 \times GF \times (QV-1) \leqq F \leqq 2 \times GF \times (QV+1)$$
$$2 \times 1000 \times (1500-1) \leqq F \leqq 2 \times 1000 \times (1500+1) \Rightarrow 2.998MHz \leqq F \leqq 3.002MHz$$

If the output voltage of an analog sensor including a temperature sensor is converted to a clock (frequency) by the VIF (Voltage to Frequency) converter using the above formula, and is input to the Ci (Io4) pin, the user can know the output voltage value of the analog sensor as a digital value.

Chapter 5 Ratings

This chapter describes the ratings of the MKY35.

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This chapter describes the ratings of the MKY35.

5.1 Electrical Ratings

Table 5-1 lists the absolute maximum ratings of the MKY35.

Table 5-1 Absolute Maximum Ratings (Vss = 0 V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 to +7.0	V
Input voltage	Vi	V_{SS}-0.3 to V_{DD}+0.3	V
Output voltage	Vo	V_{SS}-0.3 to V_{DD}+0.3	V
Output current (Co)	Iop	Peak ±12	mA
Output current (STB1,STB2,TXD,TXE)	Iop	Peak ±36	mA
Output current (Io0 to Io15, #MON)	Iop	Peak -48/+72	mA
Allowable power dissipation	PT	327	mW
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +150	°C

Table 5-2 lists the electrical ratings of the MKY35.

Table 5-2 Electrical Ratings (T_A = 25°C Vss = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{DD}	---	4.5	5.0	5.5	V
Mean operating current	$V_{DD}A$	Vi = V_{DD} or Vss Driving clock = 50 MHz output open	---	25	40	mA
External input frequency	Fclk	Input to Xi pin	---	48	50	MHz
Oscillation operating frequency	Fosc	Xi, Xo oscillator connecting	20	24 or 48	50	MHz
Oscillation feedback resistance	Rfb	V_I = V_{DD} or V_{SS} V_{DD} = 5.0 V	0.85	1.70	3.40	kΩ
Input pin capacitance	Ci	V_{DD} = Vi = 0 V f = 1 MHz T_A = 25°C	---	7	15	pF
Output pin capacitance	Co		---	7	15	pF
I/O pin capacitance	Ci/o		---	7	15	pF
Rise/fall time of input signal	T_{IRF}	---	---	---	100	ns
Rise/fall time of input signal	T_{IRF}	Schmitt trigger input	---	---	100	ms

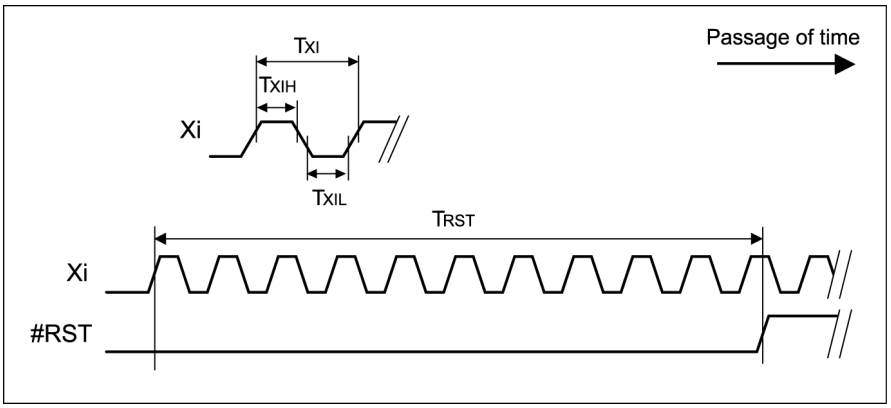
5.2 AC Characteristics

Table 5-3 lists the measurement conditions for AC characteristics of the MKY35.

Table 5-3 AC Characteristics Measurement Conditions

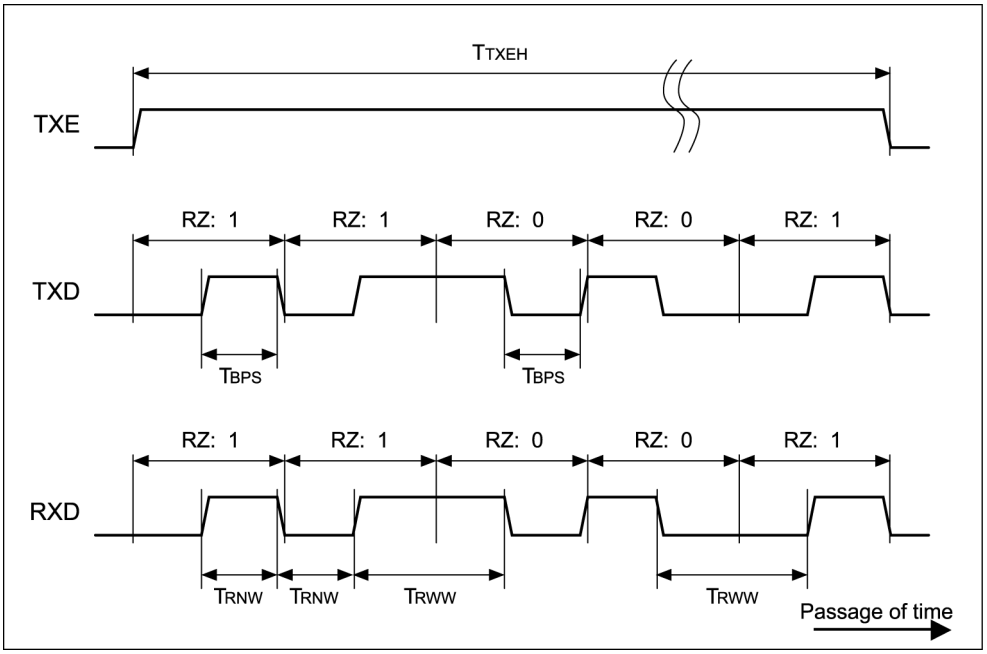
Symbol	Name	Value	Unit
COL	Output load capacitance	85	pF
VDD	Power supply voltage	5.0	V
TA	Temperature	25	°C

5.2.1 Clock and Reset Timing (#RST, Xi)



Symbol	Name	Min.	Max.	Unit
TXI	Clock period width	20	---	ns
TXIH	Clock High level width	5	---	ns
TXIL	Clock Low level width	5	---	ns
TRST	Reset enable Low level width	10 × TXI	---	ns

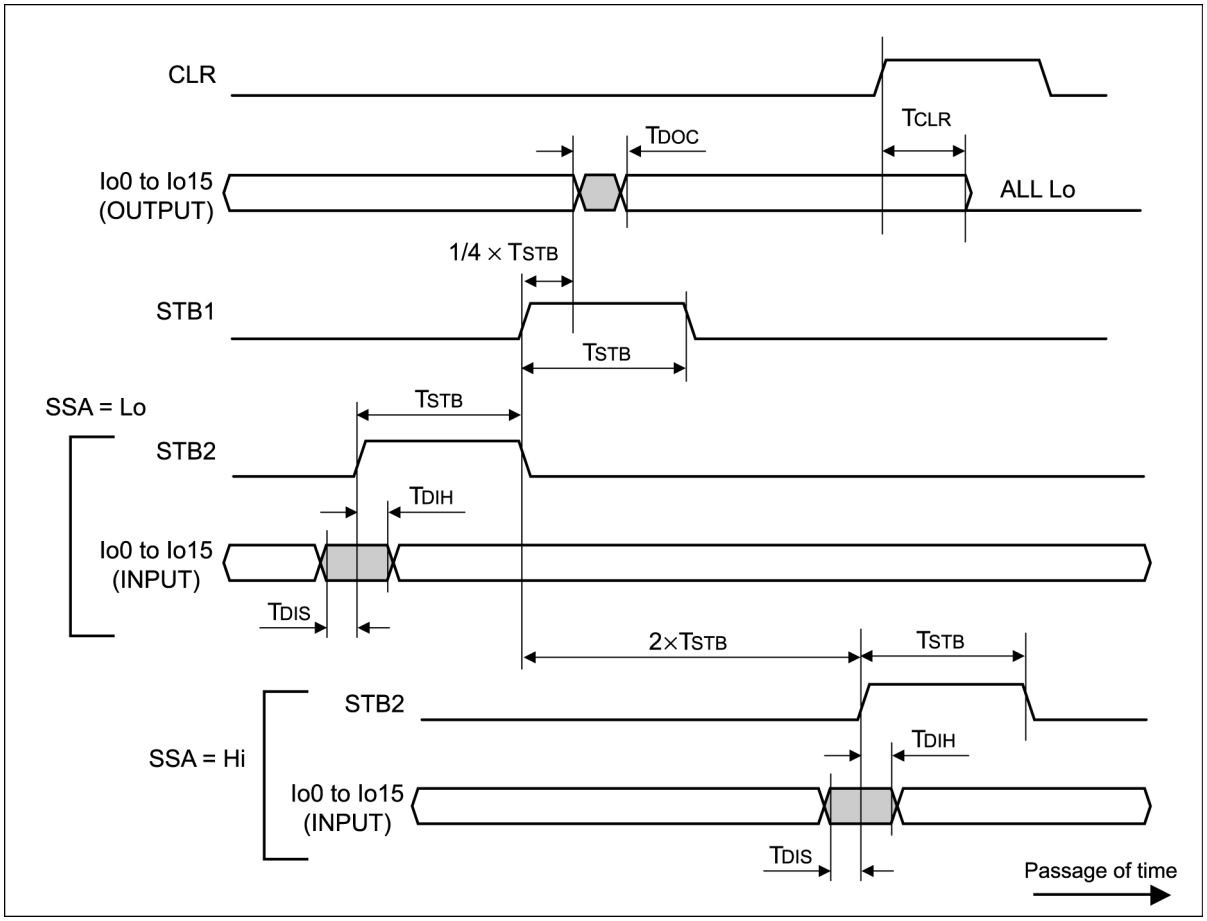
5.2.2 Baud Rate Timing (TXE, TXD, RXD)



Symbol	Baud rate	Short pulse width of sending signal	Unit
TBPS	12 Mbps	≈ 83.33 ± 5	ns
	6 Mbps	≈ 166.67 ± 5	ns
	3 Mbps	≈ 333.33 ± 5	ns

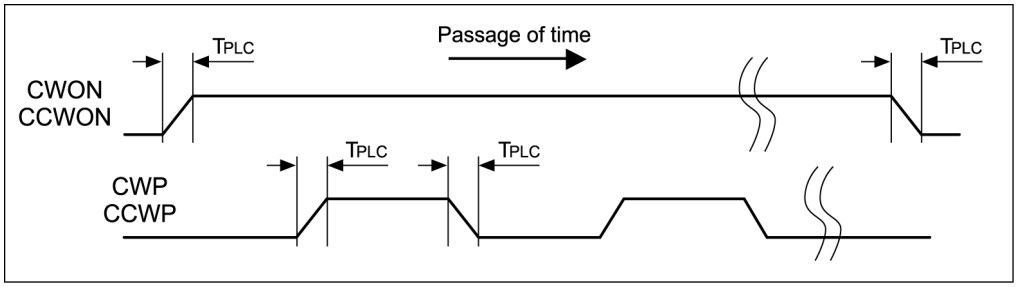
Symbol	Name	Min.	Typ.	Max.	Remarks
TTXEH	Period in which TXE pin goes High	(142 × TBPS) - 5ns	142 × TBPS	(142 × TBPS) + 5ns	--------
TRNW	Short pulse width of input signal	0.51 × TBPS	1.0 × TBPS	1.49 × TBPS	Allowable pulse width as RZ signal
TRWW	Long pulse width of input signal	1.51 × TBPS	2.0 × TBPS	2.49 × TBPS	Allowable pulse width as RZ signal

5.2.3 Strobe/I/O Pin Timing (Io0 to Io15 [in/out], STB1, STB2, CLR)



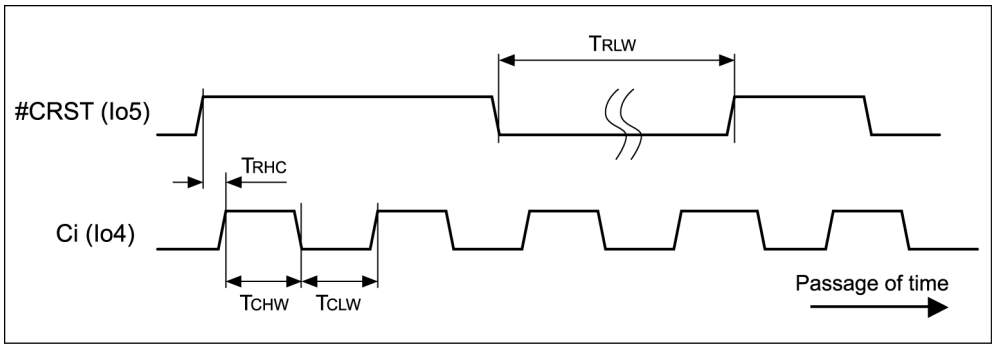
Symbol	Name	Min.	Typ.	Max.	Unit
TSTB	High-level width of strobe signal	(2 × TBPS) -5	2 × TBPS	(2 × TBPS) +5	ns
TDOC	Do data transition time	---	---	0.25 × TBPS	ns
TDIS	Di data setup	40	---	---	ns
TDIH	Di data hold	0	---	---	ns
TCLR	High-level sensing of CLR pin	0.25 × TBPS	---	0.6 × TBPS	ns

5.2.4 PWM Output Transition Timing (CWON, CCWON, CWP, CCWP)



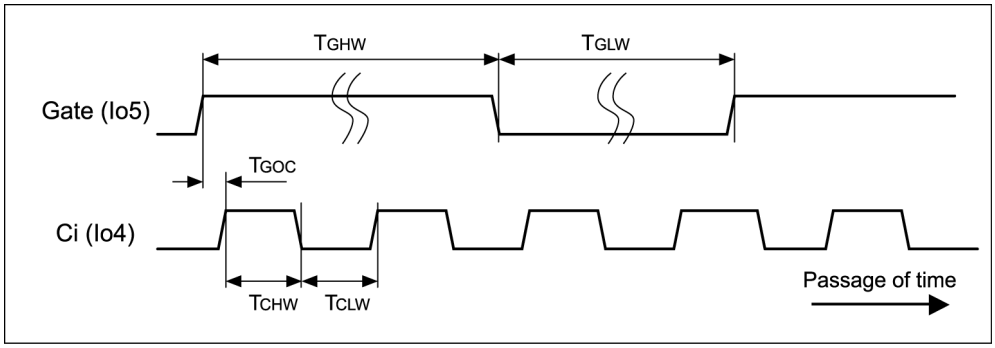
Symbol	Name	Pin load	Max.
TPLC	Level transition time	50 pF	10 ns
		100 pF	20 ns
		200 pF	40 ns

5.2.5 Universal Counter Timing (Free Count Mode: #CRST, Ci)



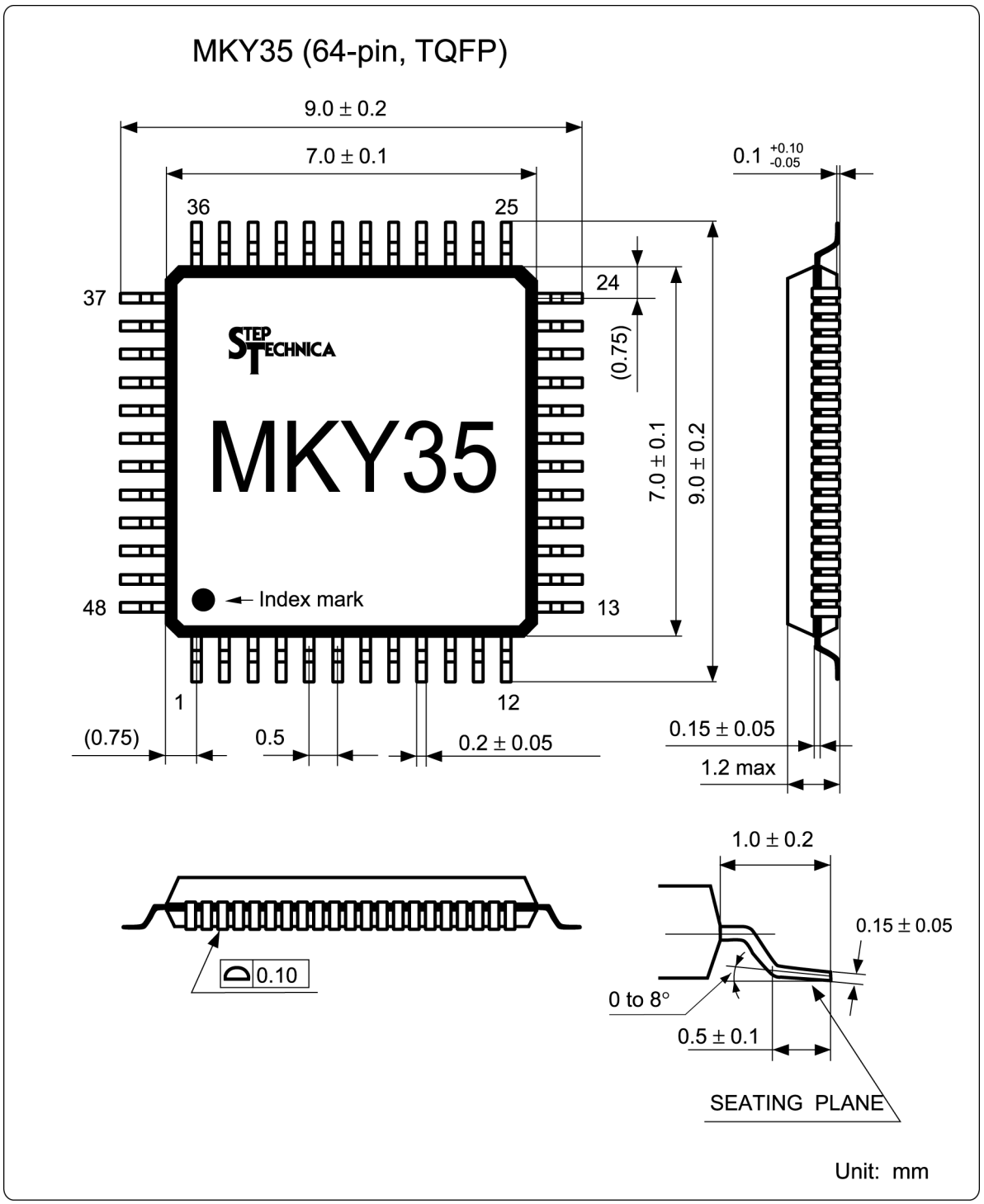
Symbol	Name	Min.	Max.	Unit
TRHC	High-level sensing of #CRSTpin	---	50	ns
TRLW	#CRST pin Low level width	2 × TBPS	---	ns
TCHW	Ci pin High level width	1.5 × TBPS	---	ns
TCLW	Ci pin Low level width	1.5 × TBPS	---	ns

5.2.6 Universal Counter Timing (External Gate Mode: Gate, Ci)



Symbol	Name	Min.	Max.	Unit	Remarks
TGOC	High-level sensing of Gate pin	---	50	ns	---
TGHW	Gate pin High level width	TBPS	---	ns	---
TGLW	Gate pin Low level width	2 × TBPS	---	ns	---
TCHW	Ci pin High level width	1.5 × TBPS	---	ns	Applies to internal gate 1 and 2 modes
TCLW	Ci pin Low level width	1.5 × TBPS	---	ns	Applies to internal gate 1 and 2 modes

5.3 Package Dimensions



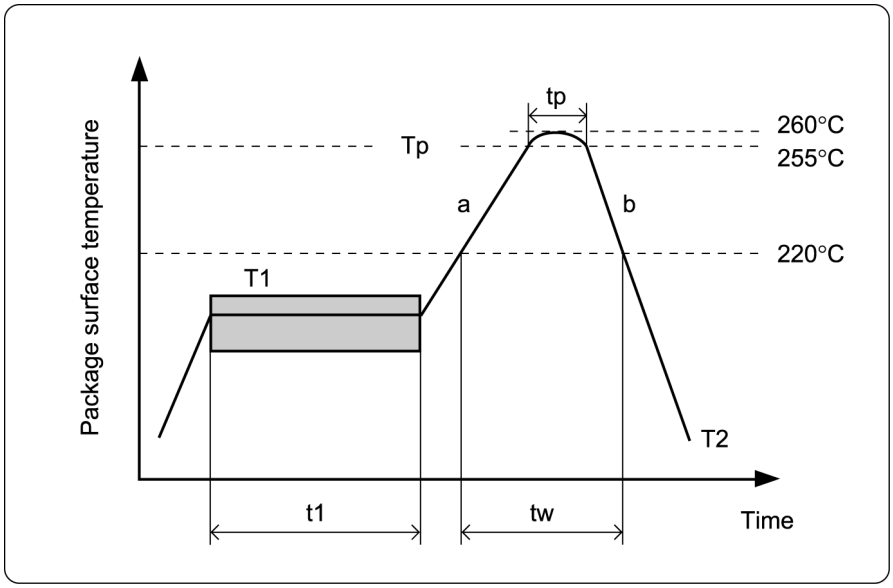
5.4 Recommended Soldering Conditions

Parameter	Symbol	Reflow	Manual soldering iron
Peak temperature (resin surface)	Tp	260°C max.	350°C max.
Peak temperature holding time	tp	10 s max.	3 s max.

Caution

(1) Product storage conditions: T_A = 30°C max., RH = 70% for prevention of moisture absorption
(2) Manual soldering: Temperature of the tip of soldering iron 350°C, 3 s max.
(Device lead temperature 270°C, 10 s max.)
(3) Reflow: Twice max.
(4) Flux: Non-chlorine flux (should be cleaned sufficiently)
(5) Ultrasonic cleaning: Depending on frequencies and circuit board shapes, ultrasonic cleaning may cause resonance, affecting lead strength

5.5 Recommended Reflow Conditions



Parameter	Symbol	Value
Pre-heat (time)	t1	60 to 120/s
Pre-heat (temperature)	T1	150 to 180°C
Temperature rise rate	a	2 to 5°C/s
Peak condition (time)	tp	10 ±3 s max.
Peak condition (temperature)	Tp	255 + 5°C
Cooling rate	b	2 to 5°C/s
High temperature area	tw	220°C, 60 s max.
Removal temperature	T2	≦ 100°C

Caution

The recommended conditions apply to hot-air reflow or infrared reflow. Temperature indicates resin surface temperature of the package.

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