STD_HLSSTU_V1.4E

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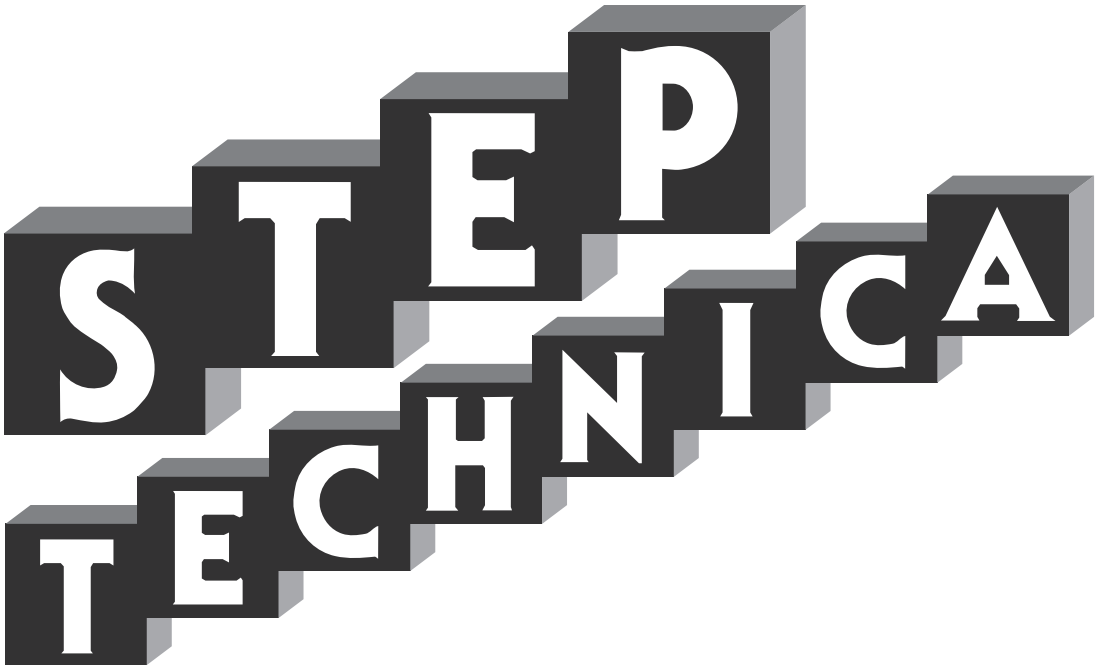

Hi-speed Link System

Introduction Guide

Note

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Preface

This manual gives an overview of the concepts of the Hi-speed Link System, and defines various terms used in the system. Be sure to read this manual before referring to each of the manuals for the various ICs comprising the Hi-speed Link System.
The Hi-speed Link System is abbreviated as HLS in this manual.

● Target Readers

This manual is for:

- Those who first build an HLS
- Those who first use StepTechnica's various ICs to build an HLS

● Prerequisites

This manual assumes that you are familiar with:

- Network technology
- Semiconductor products (especially microcontrollers and memory)

[Caution]

- ***To users with "Hi-speed Link System Users Manual" released before March, 2001***
  Some terms in this manual have been changed to conform to International Standards.

CONTENTS

Figures & Tables

1. HLS Configuration

The HLS consists of a “center IC” interfaced with the user CPU, “satellite ICs” comprising terminals, and a “network” connecting these components (Fig. 1). The network consists of “driver/receiver components (TRX)” and “cables”. Cable length can be from several centimeters to a few hundred meters. Adding “HUBs” in the network provides a high degree of flexibility in setting up topological cables, or multi-drop network offering star topology as well as point-to-point topology. In addition, cable length can be extended up to several thousand meters.

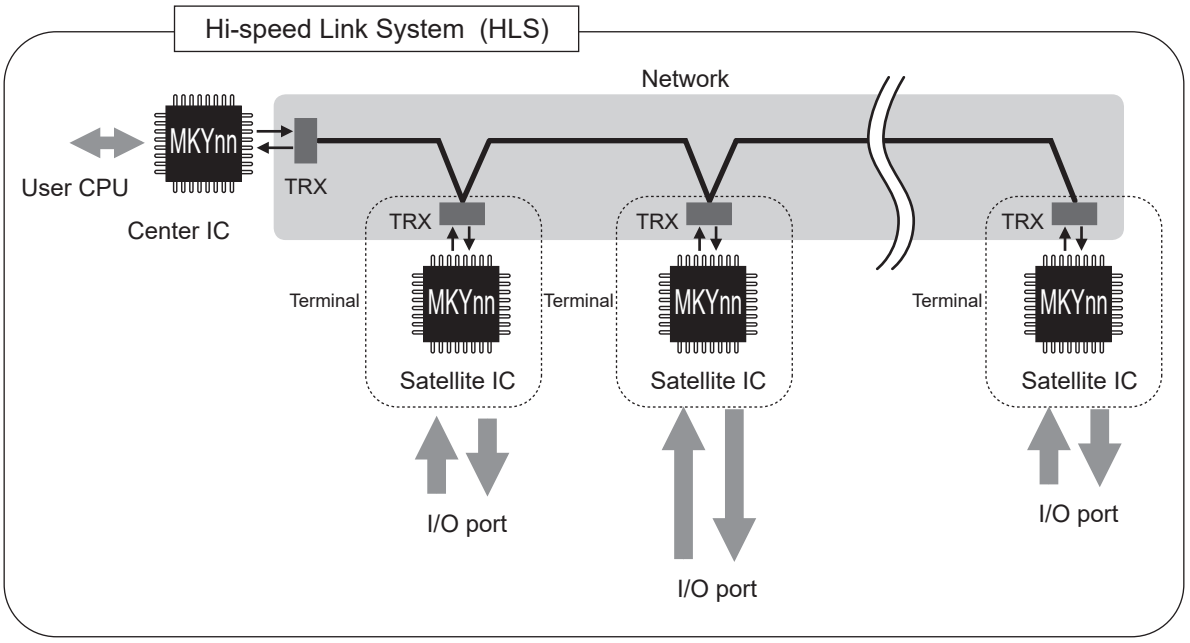

Fig. 1.1 HLS Configuration

Keyword

Center IC
User CPU
Satellite IC
Terminal
Network
HUB
Multi-drop network

2. Outline of HLS Operation

A center IC is interfaced with a bus at the user CPU, and the user CPU uses the center IC as a memory with a fixed area.
Individual Satellite Addresses (SAs) must be assigned to each satellite IC in the HLS.

The HLS copies the input port states of each satellite IC to the center IC (memory), without any auxiliary program including protocol control, from the user CPU. This copy is continually performed at a high speed by an operation described in item “6. HLS Operating Mechanism”, which allows the user CPU to arbitrarily and easily recognize the state of the input ports of all satellite ICs just by reading any address of the center IC (memory).

The HLS individually copies data in the center IC (memory) to the output port of each satellite IC, without any auxiliary program including protocol control, from the user CPU.
This copy is also continually performed at a high speed by the operation described in item “6. HLS Operating Mechanism”, which allows the user CPU to arbitrarily and easily set the state of the output ports of all satellite ICs just by writing data to any address of the center IC (memory).

Keyword **Memory**
SA (Satellite Address)

3. HLS Use and Effects

The HLS enhances CPU resources based on an entirely new concept that is designed to easily set up a huge memory-mapped remote I/O. Adopting the HLS to devices or systems controlled by a CPU offers the following advantages:
(1) Fewer signal cables → Less wire
(2) Lower maintenance cost → Less work load
(3) Smaller footprint → Lower production cost
(4) Shorter and simpler development procedure → Lower development costs
(5) Unitized and standardized functions → Shared technology

The HLS contributes to automation in many industries, such as precision machine tools, industrial equipment including instrumentation and control systems, robots, research facilities, building administration systems, and conveyer systems.

Keyword **Enhances CPU resources**
Huge memory-mapped remote I/O

4. Actual HLS Operation (Specific Example)

Specific examples of actual HLS operation are shown below.

4.1 Retention of Same Data

In the HLS, the bit state of the center IC memory is always the same as the I/O state of the remotely-placed terminal unit with the satellite IC.

- For example, writing 135AH to memory address 082H, the output pins of the remote terminal 100 m away reflect 135AH (Fig. 4.1), retaining the same data.
- For example, reading memory at address 102H when the state of input pins of the remote terminal 100 m away read 79C4H, the center IC memory can also read 79C4H, what is the same state as the input pins of the remote terminal (Fig. 4.1).

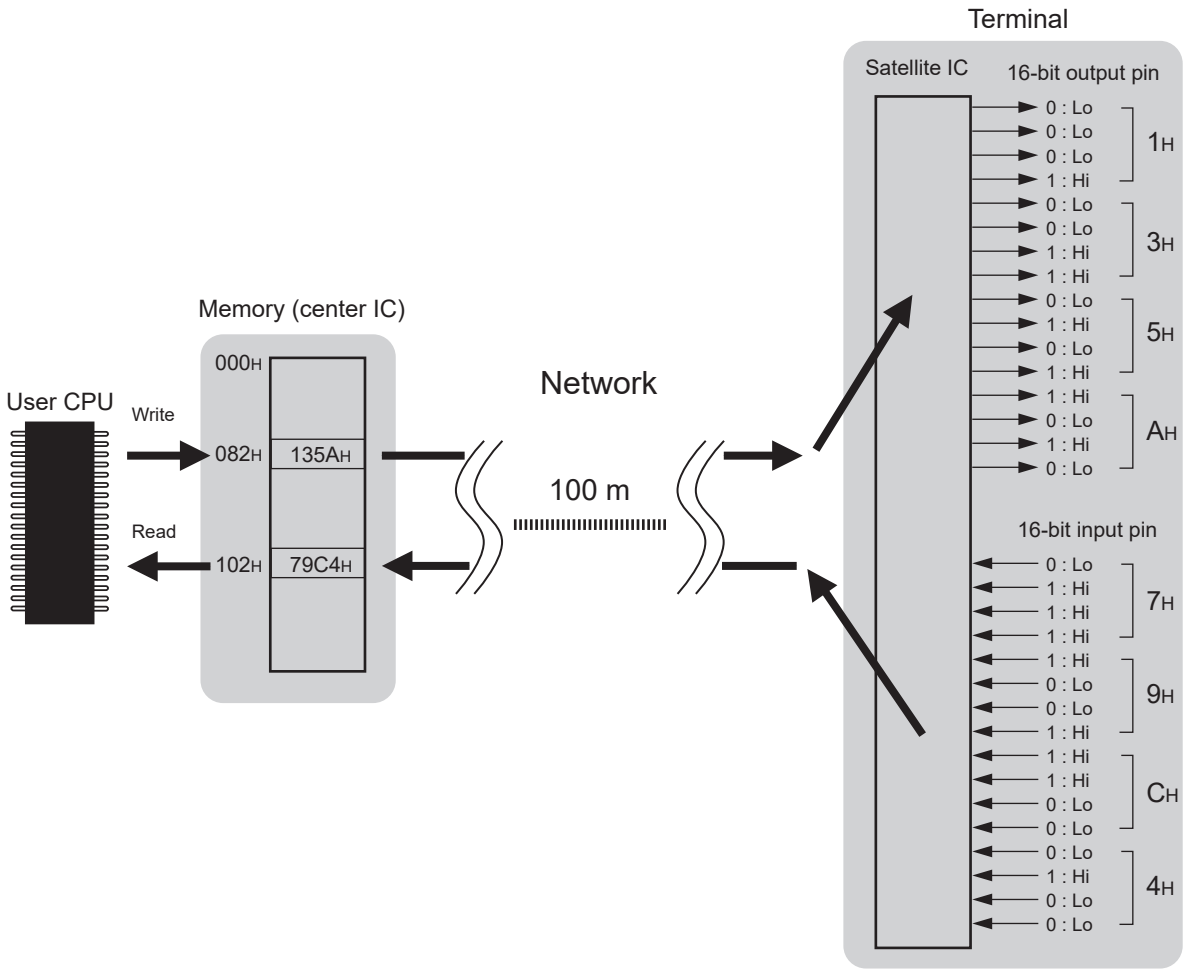

Fig. 4.1 Center IC Retaining Same Data

4.2 Number of Terminals

The HLS is designed to connect up to 63 terminals.

- For example, when memory address 102H is read when data of the input pins of the first remote terminal 70 m away read 9876H and data of the input pins of the second remote terminal 100 m away is 1234H, the same data (9876H) as the input value of the first terminal can be read. Similarly, when memory address 104H is read, the same data (1234H) as the input value of the second terminal can be read (Fig. 4.2).

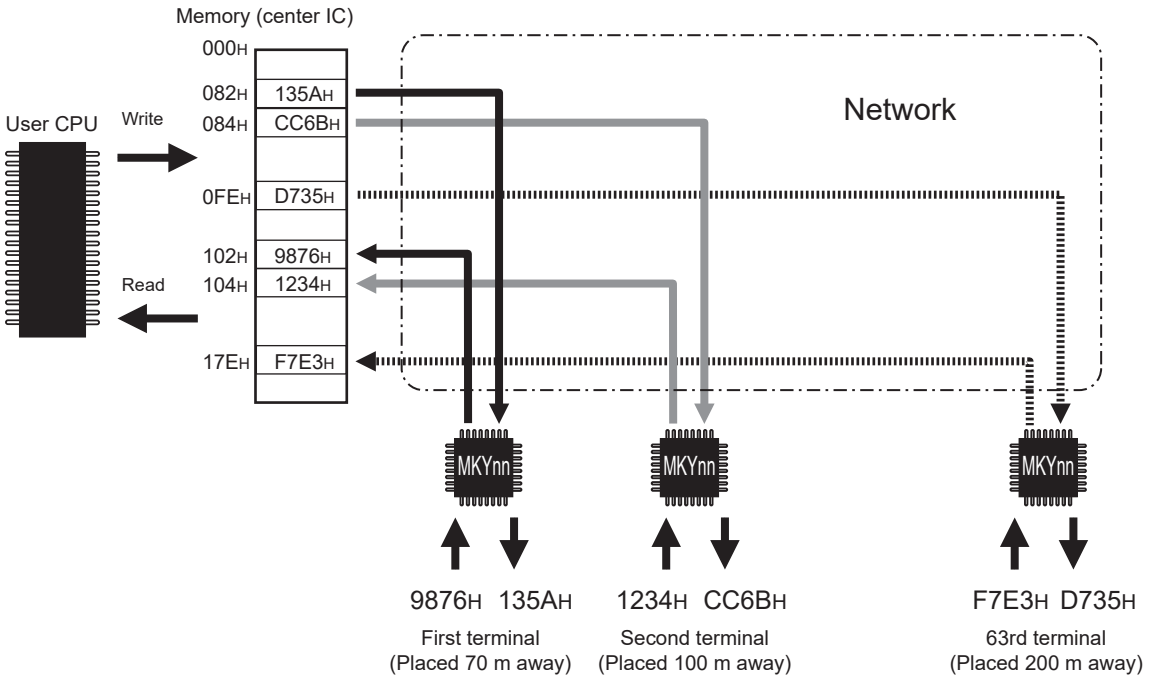

Fig. 4.2 Connection of Multiple Satellite ICs

4.3 Number of Cables

Only one cable is used for connecting the center equipment and each satellite terminal in the HLS (Fig. 4.3). The HLS consists of one center equipment and multiple satellite terminals. The center equipment can be multi-dropped to multiple terminals on a network cable. Using this simple connection, a user can build a network easily even though the network cable length is 100 m or more (, requiring no advanced knowledge on analog signals and signal propagation).

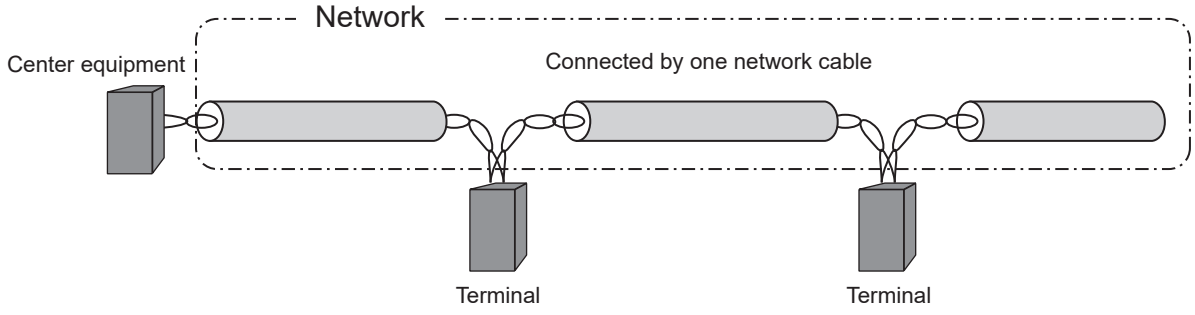

Fig. 4.3 Connection between Center Equipment and Terminals

4.4 Origin of HLS

[Constancy: Always stays the same]

The main feature of the HLS is that “constancy” and “real-timeness” are assured.
To represent this feature, the system including the center IC series and satellite ICs series comprising the HLS was named “Hi-speed Link System”.
The HLS always scans the memory bit state and the I/O state of network-linked terminals automatically.
The time to completely execute one scan cycle is called the “scan time”.
The scan time is calculated arithmetically; it is assured and does not fluctuate.

Keyword **Constancy (always stays the same) and real-timeness are assured Scan time**

4.4.1 Constancy

A typical example of HLS is shown below.
If “constancy” is not maintained in a system where the digital outputs of the sequential-transformation A/D converter are connected to the input pins of the terminal, distorted analog data waveforms are supplied to the center IC memory. In contrast, the HLS “constancy” is maintained so that the center IC memory is updated with the latest analog data at regular intervals. The HLS allows copying of undistorted analog data (Fig. 4.4).

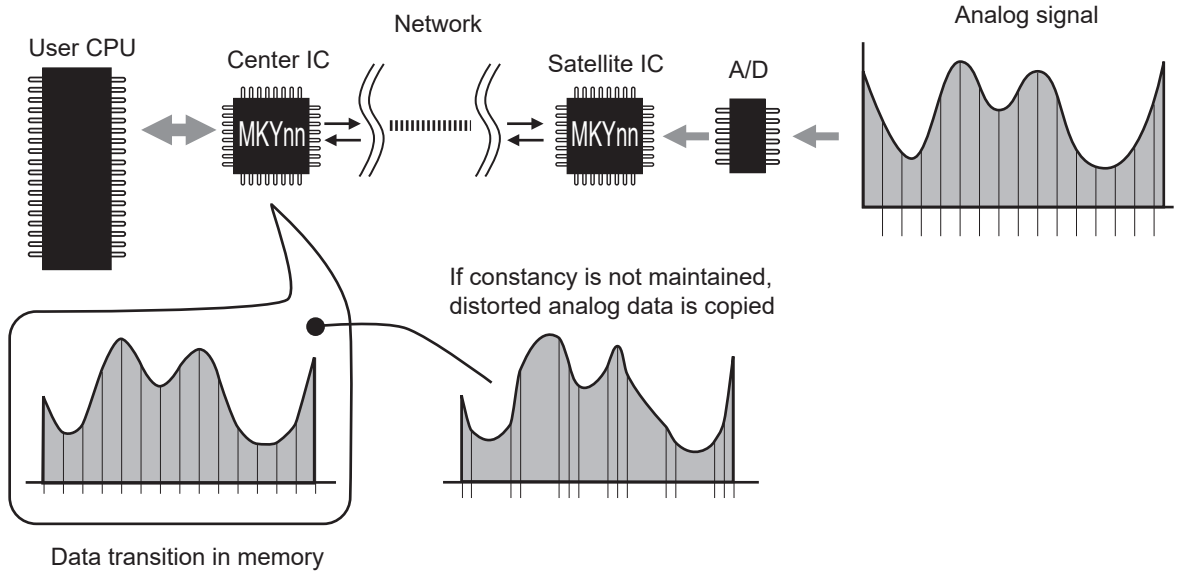

Fig. 4.4 Constancy

4.4.2 Real-timeness

A typical example of HLS real-timeness is shown below.
In a system with three pass sensors at 30-cm intervals in line connected to the terminal input pins, even if an object passes the sensors at the breakneck speed of 1000 km/h, the data in the center IC memory will still transit accordingly. For example, if a meteorite passes through sensors at a speed of 1000 km/h, the user CPU can recognize the meteorite's passage based on the data transition in the center IC memory (Fig. 4.5). As can be seen from this example, the HLS can be used for user system requiring extremely high "realtimeness".

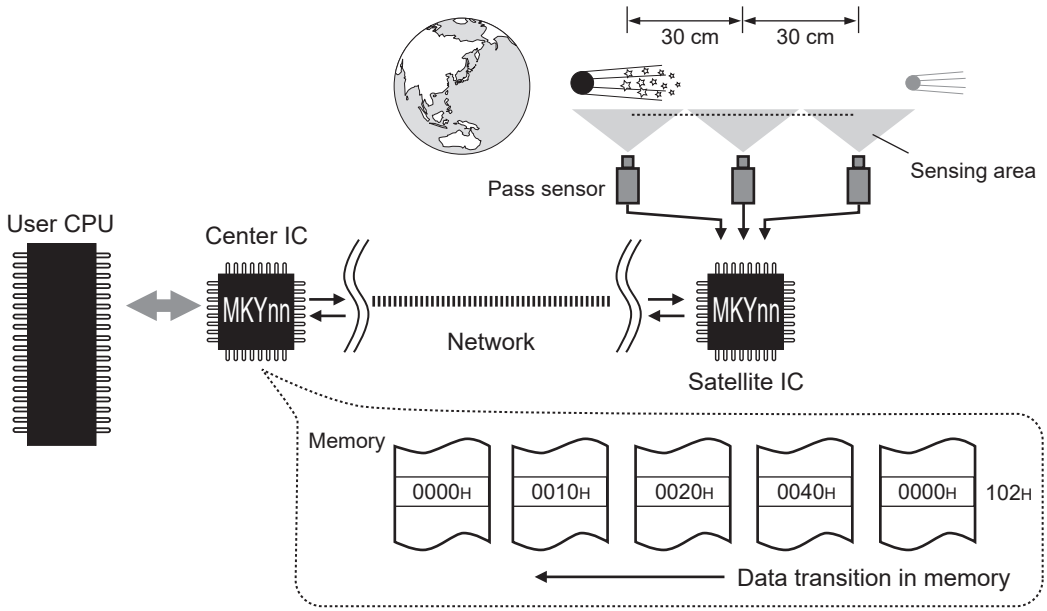

Fig. 4.5 Real-timeness

4.5 HLS in Various Control and Instrumentation Systems

"Constancy" and "real-timeness" are assured for output signals of a terminal controlled by a user CPU.
For example, the scan time in the HLS, which can scan 63 terminals, is 955.5 µs (12 Mbps in full-duplex mode), and each terminal can use 16-bit signal inputs and 16-bit signal outputs. Thus, in the total number of input signals (1008) and output signals (1008) of 63 terminals, a consistent response time of 955.5 µs can be maintained.

With these features, the HLS has many applications in building various control and instrumentation systems.

5. Outline of HLS Components

The HLS consists of a center IC, satellite ICs, and a network.

5.1 Center IC

- The center IC is connected to the user CPU by the address bus and data bus, and the chip select (CS), read (RD) and write (WR) control lines of the user CPU. The user CPU can handle the center IC as a simple memory (Fig. 5.1).
- User system can operate the HLS just by having read access and write access to registers and areas allocated to memory.

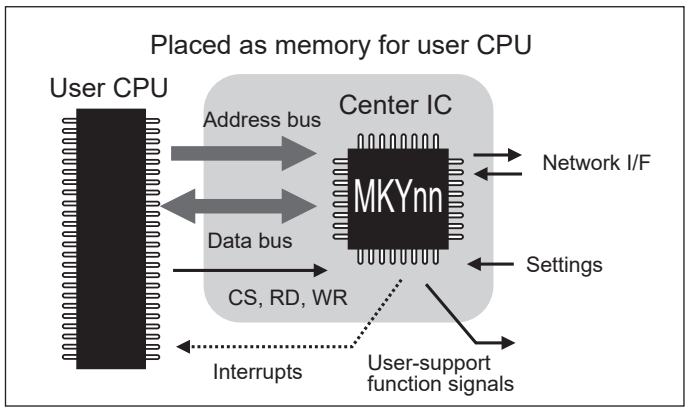

Fig. 5.1 Center IC

- The center IC has a network interface (“network I/F”). It also has user-support functions, such as setting pins, pins to generate interrupt triggers to the user CPU, and LED pins to display the HLS operating condition.

Keyword

Network I/F
User-support function
Setting pin

Reference For details of how to connect to the user CPU, registers and areas allocated to memory, and user-support functions, refer to each “Center IC Manual”.

5.2 Satellite IC

- In the HLS, an IC comprising a terminal is called a “satellite IC”.
- The satellite IC has a network I/F, 16 input pins, and 16 output pins (Fig. 5.2). Some satellite ICs have combined 16 input and 16 output pins.
- The satellite IC has SA (Satellite Address) setting pins to identify multiple terminals. Each satellite IC in one HLS must be assigned an individual SA.
- In addition to simple input/output functions, some satellite ICs have expanded functions for system integration.

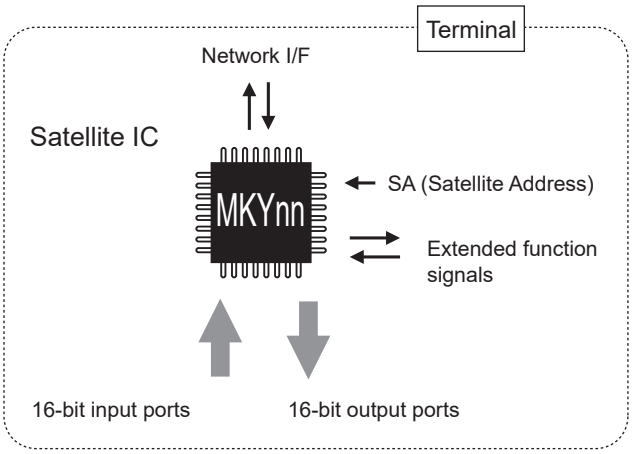

Fig. 5.2 Satellite IC

Reference For details of the specific functions and how to use satellite IC, refer to each ***“Satellite IC Manual”***.

5.3 Network

- The HLS can be used with many types of the network cables or communication modes.
- The HLS can operate on any network allowing transmission of signals from the network I/F of the center IC to the satellite IC, or the transmission of signals from the network I/F of the satellite IC to the center IC.
- "Half-duplex" and "full-duplex" communication modes can be selected for the HLS.
- For simplicity and reliability, StepTechnica recommends the connection in Figure 5.3. The recommended networks are as follows:
  - TRX (driver/receiver) consists of differential driver/receiver (based on RS-485) components and pulse transformer (for electrical isolation)
  - Ethernet LAN cable rated "Category-3" or higher

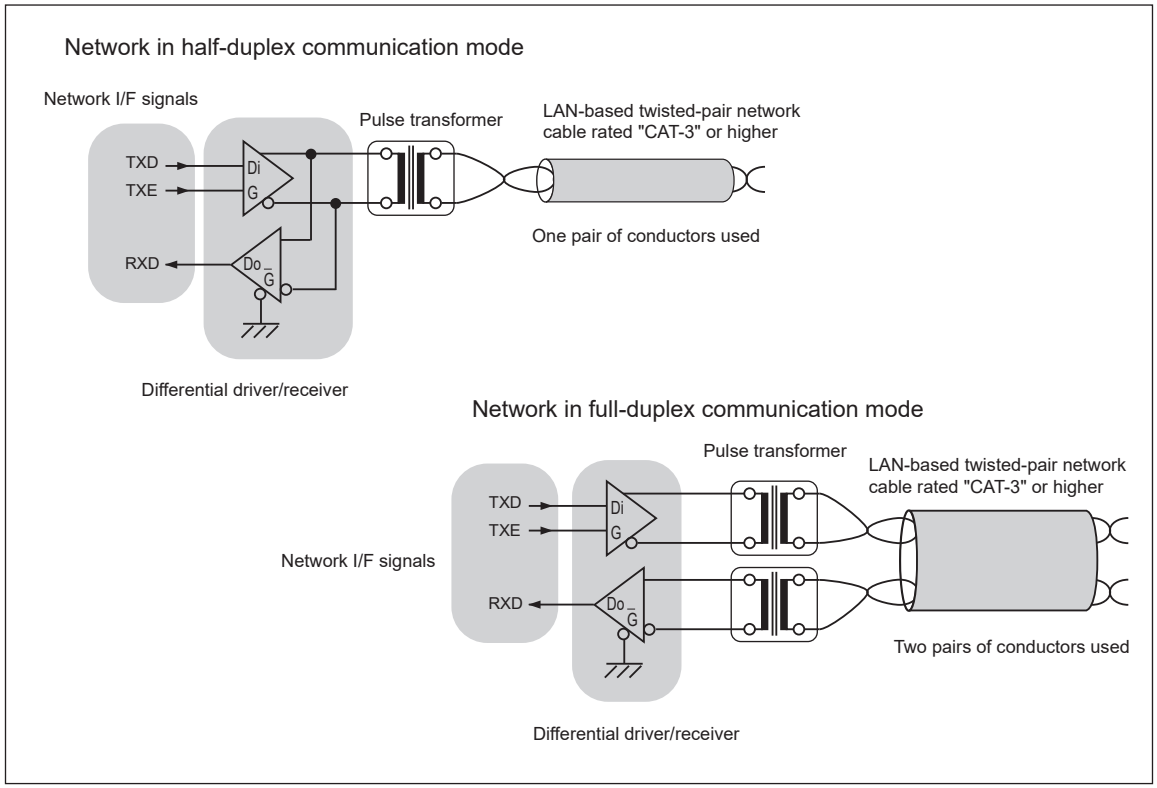

Fig. 5.3 Network

Keyword

Network cable
Communication mode
Half-duplex
Full-duplex
TRX consists of differential driver/receiver components and pulse transformer

Reference

Background information to help build a network are described in ***"Hi-speed Link System Technical Guide"***. For more information about how to select components or to get recommended components, visit our Web site at www.steptechnica.com/en/.

6. HLS Operating Mechanism

- In the HLS, automatic scanning between the center IC and satellite ICs is performed constantly by a serial pattern format command packet (CP) and response packet (RP) tailored specifically for the HLS.
- When operating the HLS, select either half duplex or full duplex as the communication mode and set the mode in the center IC. Connect the network based on the communication mode.
- Figure 6.1 shows the transfer of the CP and RP in half-duplex mode on the network based on the passage of time. This indicates actual scanning in the HLS. The details are explained below.

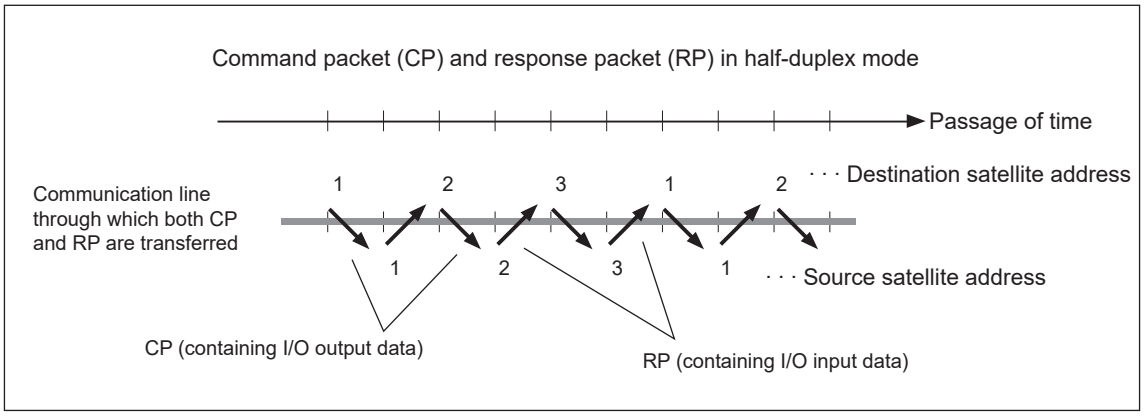

Fig. 6.1 Transfer of CP and RP in Half-duplex

(1) To operate the HLS, set (write) the Final Satellite (FS) scanning value to the given register in the center IC from the user system. Figure 6.1 shows an example of starting the operation of the HLS by writing "3" (03H) as the FS to the center IC.

(2) The center IC sequentially sends the CP from "SA = 1" to "SA = FS" to the satellite IC at regular intervals, that are repeated automatically. This CP contains data which is in the address corresponding to the SA that sends the CP in the center IC (memory).

(3) When the satellite IC receives the CP sent to its own SA, it updates the state of the output port based on this CP, and immediately returns the RP containing the state of the input port as data to the center IC. The CP and RP appear regularly one after the other on the network as shown in Figure 6.1.

(4) When the center IC receives the RP from the satellite IC, it updates the data in the center IC (memory) for the address corresponding to the SA that sent the RP to the latest received data.

(5) Automatically repeated scanning and updating causes the bit state in memory controlled by the center IC to be the same as the I/O state of the remote terminal. In this operation, both constancy and realtimeness are assured.

■ Figure 6.2 shows the transfer of the CP and RP in the full-duplex mode on the network based on the passage of time. In full-duplex mode, each CP and RP propagates through a dedicated communication line, which enables the center IC to receive a RP while sending the next CP. Therefore, the CP sending interval is shortened, resulting in a faster scan time.

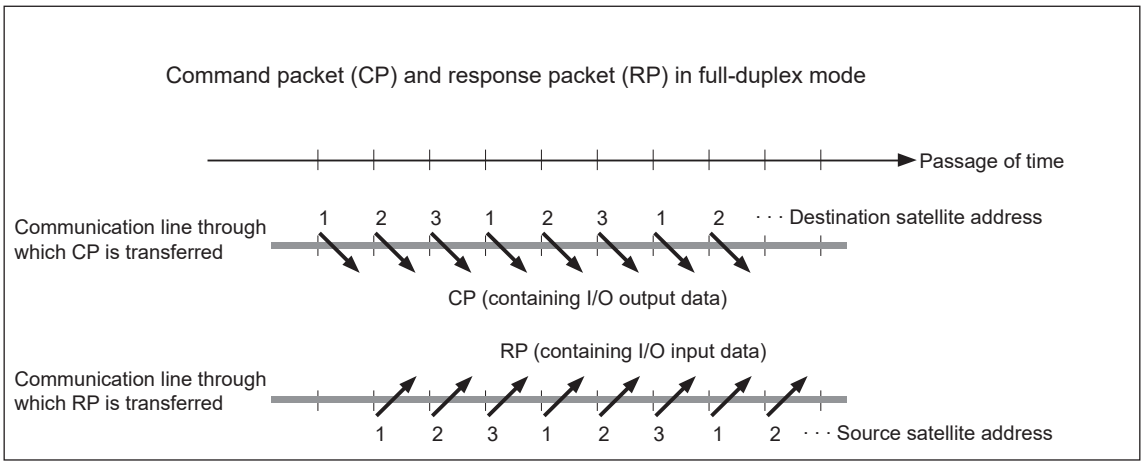

Fig. 6.2 Transfer of CP and RP in Full-duplex

Caution The HLS serial pattern format is exclusive to the HLS and cannot be used with other serial communication types, such as RS-232C and Ethernet LAN.

Keyword **Final Satellite (FS)**

7. Baud Rate of HLS

- The HLS CP and RP consist of two values (Hi and Lo of a given width) of RZ (Return to Zero or "Manchester code") that function in pairs (Fig. 7).
  In the HLS, the "baud rate" refers to the bps (bits per second) unit representing how many time widths of the smallest unit (one Hi level or one Lo level) making up one pair occur in 1 second. One Hi-level or Lo-level time width is expressed as "TBPS".
  For example, if the baud rate is "10 Mbps", the time width TBPS is 100 ns, indicating that 10,000,000 Hi-level and Lo-level pulse signal strings are propagated over the network in 1 second.

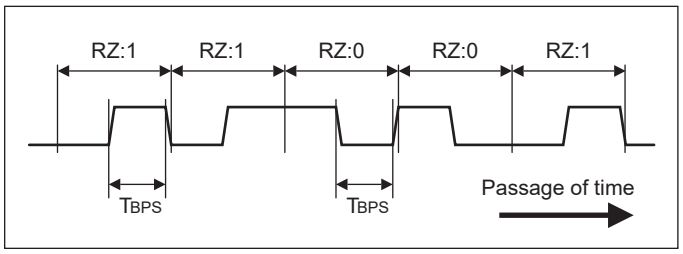

Fig. 7.1 RZ (Return to Zero) Comprising CP and RP

- In the HLS, the recommended baud rates are "12 Mbps", "6 Mbps", and "3 Mbps". These baud rates are usually selected depending on the network length (network cable length) (Table 1).

Table 1 Baud Rates and Network Cable Lengths

Baud rate	Network cable length	TBPS
12 Mbps	to 100 m	≈ 83.33 ns
6 Mbps	to 200 m	≈ 166.67 ns
3 Mbps	to 300 m	≈ 333.33 ns

Each connection point of a multi-drop network cable is called a "branch". Table 1 indicates the network cable length for the HLS when using the network with 32 or less branches.
The recommended differential driver/receiver is an RS-485-based driver/receiver. Therefore, the branch count "32" stipulated in the RS-485 specification is used as a guide in Table 1.
Up to 63 HLS satellites can be connected to the HLS, enabling connection of "63" branches. This recommended network is isolated electrically by a pulse transformer and the format of signals propagated through the network is RZ (Return to Zero). Consequently, "63" branches can be connected using a standard RS-485-based driver/receiver without using DC component signals. In this case, the cable length is likely to be shorter than the value in Table 1 (due to increase of dispersion of propagated signal energy).

Caution The network cable lengths in Table 1 are provided as a guide for each baud rate, but performance is not guaranteed.

Reference The baud rates and background information to help build a network are described in ***"Hispeed Link System Technical Guide"***.

Keyword
RZ (Return to Zero or "Manchester code")
Baud rate
TBPS
Network cable length

8. HLS Scan Time

The HLS scan time is assured to stay constant (constancy).
This scan time can be calculated from an equation based on the following three determinants:
(1) Full-duplex or half-duplex communication mode
(2) Final Satellite (FS) values that the user system wrote to registers in the center IC
(3) Baud rates

■ The equation for scan time in full-duplex mode is shown below.

$$182 \times FS \times T_{BPS}\ (s)$$

Note: "182" is a constant.

■ The equation for scan time in half-duplex mode is shown below:

$$354 \times FS \times T_{BPS}\ (s)$$

Note: "354" is a constant.

Reference In common serial communications, such as RS-232C and Ethernet LAN, if a communication error is caused by external noise during packet transmission, communication retries are commonly made. In these communication modes, communication stops unless a retry is made. In contrast, the HLS always performs periodic scanning so if a communication error is caused by external noise during packet transmission, the next scanning is equivalent to a retry. Therefore, retry is not made in the HLS.

Table 2 shows typical scan times (reference values) calculated by the above equations.

Table 2 Typical Calculated Scan Time Values

FS value	12 Mbps		6 Mbps		3 Mbps	
	Full-duplex	Half-duplex	Full-duplex	Half-duplex	Full-duplex	Half-duplex
4	60.7 µs	118.0 µs	121.4 µs	236.0 µs	242.7 µs	472.0 µs
8	121.4 µs	236.0 µs	242.7 µs	472.0 µs	485.4 µs	944.0 µs
16	242.7 µs	472.0 µs	485.4 µs	944.0 µs	970.7 µs	1.888 ms
32	485.4 µs	944.0 µs	970.7 µs	1.888 ms	1.942 ms	3.776 ms
48	728.0 µs	1.416 ms	1.456 ms	2.832 ms	2.912 ms	5.664 ms
63	955.5 µs	1.859 ms	1.911 ms	3.717 ms	3.822 ms	7.434 ms

Caution When you insert a hub into the network or the user system pauses a scanning, you must use different equation to calculate scan time. For details, refer to each ***"Center IC Manual"***.

9. Copied Data Quality Guarantee

The HLS guarantees the copied data quality.

9.1 Tests at Packet Reception

The HLS performs the following three tests concurrently when receiving packets. This prevents the garbage data that occurs in other communications.

(1) **Pattern format test:** This test examines whether the pattern format of the command paket (CP) and response packet (RP) meets an HLS-dedicated serial pattern format starting with a specific pattern at the completion of packet reception.

(2) **CRC-12 test:** Generally, in an Ethernet LAN and bulk communications, one "CRC-12" block check code (BCC) is used for an array of thousands to tens of thousands of bits. In contrast, the HLS uses a CRC-12 BCC for one packet (containing less than several hundred bits). This BCC is examined at the completion of packet reception.

(3) **Validity test of RZ signal format (RZ test):** The HLS command packet (CP) and response packet (RP) consist of pulse arrays for RZ (Return to Zero or "Manchester code") described in item ***"7. Baud Rate of HLS"***. The HLS examines received packets in bit units to check that the RZ format is maintained.

Reference Generally, although the "test" and "correction" concepts are used in serial communications, "correction" is completely different from "test". "Correction" restores damaged packets. It is effective if data like consecutive voice data is permitted to have a certain error level (garbage data). However, it is not suitable for the HLS. The HLS performs only "tests" and discards all received packets failing the tests.

9.2 Link Management and Handshake for Individual Satellite ICs

In the HLS, the normal reception of the RP from the satellite IC after sending the CP is called "link". The center IC always manages the individual link status of each satellite IC, and the link status is indicated by specific bits in memory.

By referencing the individual link status of all satellite ICs to be scanned, the user system can get assure that memory data in the center IC is the same as the I/O state of the satellite IC.

Some satellite ICs have a handshake function that does not allow the input of new data if the center IC does not receive any RP.

Keyword

Perform three tests concurrently
Pattern format test
CRC-12 test
Validity test of RZ signal format (RZ test)
Link
Always manages individual link status
Handshake

10. Other HLS Features

The HLS provides the following features and benefits based on practical know how by covering system development and maintenance, such as examination of communication environments, installation of user system and network cabling, and detection of network failures and errors, as well as signal copy.

(1) The center IC of the HLS is designed to be connected all types of satellite IC, and those satellite ICs can be mixed together.
(2) The HLS terminals can connect to and disconnect from the network even if the HLS is in operation.
(3) The HLS always manages communication errors resulting from external noise during scanning, improper environments, or system failures. Even if an unexpected error occurs, the user can easily detect the error.
(4) The user can easily detect the state transition in terminals comprising the HLS and connected or disconnected terminals using the registers and flag bits in the center IC.

11. Precautions for Actual Use of HLS

This manual describes the basic concept of the HLS for the center IC and satellite ICs comprising the HLS network.

When actually using the HLS, it is important to understand the functions and performance by referring to ***"Center IC Manual"***, ***"Satellite IC Manual"***, and ***"Hi-speed Link System Technical Guide"***.

Manual update information, product information, technical reports, etc., will be available in the near future at our Web site:

https://www.steptechnica.com/en/

Revision History

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1.4	March, 2023		typographical error correction

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