DS_MKY44AD12A_V1.4E

STEP TECHNICA CO.,LTD.

CUnet Family

MKY44-AD12A

DATA SHEET

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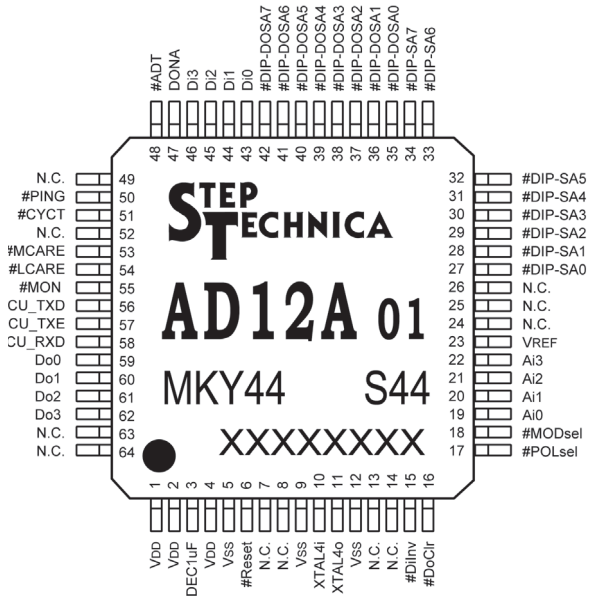
MKY44 Series CUnet-Compliant Intelligent Slave ICs

key words : 4ch 12 bits A/D 4 bits DI 4 bits DO

CUnet

■ MKY44-AD12A Specifications

- ● Model : MKY44-AD12A
- ● ADC : Built-in
- ● Analog input range : 0 V to VREF
- ● A/D conversion resolution : 12 bits
- ● A/D conversion time : approx. 26 μs/conversion (internal)
- ● Non-linearity error : ±3 LSB
- ● Number of channels : 4-channel multiplexer
- ● Reference voltage : 2.2 V to 3.3 V
- ● Loading mode
  - • Cyclic mode
  - • Single trigger mode (software trigger or hardware trigger)
  - • Moving average mode
  - • Period average mode
- ● Parameter settings for moving average mode and period average mode
  - • Sampling frequency (2 times, 4 times, 8 times, or 16 times)
  - • Sampling cycle (200 μs to 1 s, in units of 100 μ)
  - • Peak cut
- ● DIO : 4 bits DI/4 bits DO
- ● Power voltage : 3.3 V
- ● Power consumption : 20 mA
- ● Temperature range : -40 to +85 °C
- ● Package : 64-pin TQFP (0.5 mm pitch 10 mm × 10 mm)
- ● ST44SW : Not required



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

■ Applications

Industrial devices
Medical devices
Measurement devices
Power wire monitoring
Process control

■ Overview

The MKY44-AD12A is a CUnet station IC with analog input function. With an MKY44-AD12A, analog input control and DIO control can be achieved on one chip without using the CPU. For analog input, the data acquisition timing can be selected from 4 modes. There are also parameter settings for smoothing processing. Measurement data according to the set mode is automatically input to the MKY44-AD12A's own memory block. The input data is automatically copied to all CUnet ICs through CUnet communication (memory sharing), so the user CPU can acquire analog data easily just by reading the memory blocks corresponding to each slave IC. Existing users of CUnet can get analog control just by adding this product to their networks. New users have the opportunity to reduce A/D control wiring that used to use parallel connections and to achieve easy, networked analog control.

■ Four Sampling Methods

A/D conversion in the MKY44-AD12A includes A/D conversion of the analog input of ch0, followed by A/D conversion of the analog input of ch1, ch2, and ch3. The difference of sampling time for each channel (ch) is approximately 26 μs. The selected sampling method is shared in all channels from ch0 to ch3. For period average and moving average, you can set the sampling cycle and sampling frequency. You can also specify peak cut of the maximum value and the minimum value.

- Cyclic mode: CUnet executes communication regularly (cyclically). When "cyclic mode" is selected as the sampling method, the chip will execute A/D conversion for each cycle of CUnet and store the latest analog value in its occupied area (henceforth "self-owned area") within the shared memory of CUnet. The cycle time of CUnet communication is a constant value depending on transfer rate and other factors. For example, the cycle time is 155 μs in a system with 4 nodes at 12 Mbps.

- Single trigger mode: In single trigger mode, there are "hardware trigger mode" and "software trigger mode." If hardware trigger mode is selected, the MKY44-AD12A will execute A/D conversion when a bit selected from bits Di0 to Di3, which correspond to the four general-purpose input pins, transits from "1" to "0," and it will store the analog value in the shared memory. If software trigger mode is selected, the master MKY43 can set the trigger data and address for the MKY44-AD12A. The chip will execute A/D conversion and store the analog value in its self-owned area when the data of that address transits to the specified data.

- Period average mode: For the sampling interval, you can set 200 μs to 1 s. For the sampling frequency, you can set 2, 4, 8, or 16 (4, 6, 10, or 18 when in peak cut). The MKY44-AD12A stores in the self-owned area the average value of A/D conversion data corresponding to the predetermined sampling interval and sampling frequency. The factory default sampling interval is 1 ms (1 kHz). The factory default sampling frequency is 8 times. With these settings, the interval at which the period average data is updated in the self-owned area is 8 ms "without peak cut" of the maximum and minimum values and 10 ms "with peak cut."

- Moving average mode: The MKY44-AD12A stores in the self-owned area the moving average value of the A/D conversion data corresponding to the predetermined sampling interval and sampling frequency. The sampling interval and frequency are the same as in period average mode. With the factory default settings (sampling interval 1 ms, sampling frequency 8 times), the interval at which the moving average data is updated in the shared memory is 1 ms, the same as the sampling interval.

Note: If period average or moving average mode is selected, the MKY44-AD12A will not participate in the network until the first average data is generated after returning from a reset. In such a case, the chip might take as long as 18 seconds before participating in the network depending on the settings for peak cut, sampling frequency, and sampling interval.

Note: If the sampling interval is set to 200 μs in the MKY44-AD12A, the values to which sampling frequency can be set will be limited.
When "with peak cut," the sampling interval can be set to 200 μs if the sampling frequency is 2 or 4 times.
When "without peak cut," the sampling interval can be set to 200 μs if the sampling frequency is 2, 4, or 8 times.

■ Data Placement of the Occupied Memory Block

The MKY44-AD12A occupies one MB (memory block) corresponding to the specified SA value. The MB occupied by the MKY44-AD12A is 8 bytes (64 bits). The data configuration within the 8 bytes is as follows.

Address	0x07		0x06		0x05		0x04		0x03		0x02		0x01		0x00	
bit	63 to 60		59 to 48		47 to 44		43 to 32		31 to 28		27 to 16		15 to 12		11 to 0	
	SN		ch3 Analog Value		Status		ch2 Analog Value		Status		ch1 Analog Value		Di		ch0 Analog Value	
bit	63	62	61	60	47	46	45	44	31	30	29	28	15	14	13	12
	SN3	SN2	SN1	SN0	Stype1	Stype0	MODsel	“0”	TRGsel	DiInv	PCsel	POLsel	Di3	Di2	Di1	Di0

When other devices connected to CUnet need to refer to the input value of the analog input terminal with the MKY44-AD12A, they can simply read the memory block occupied by the MKY44-AD12A. Details follow.

(1) To refer to the analog value of ch0, read bits 11 to 0. To refer to the analog value of ch1, read bits 27 to16.
To refer to the analog value of ch2, read bits 43 to 32. To refer to the analog value of ch3, read bits 59 to 48.
Since the data is in little endian format, lower bits represent lower address positions. Whether these values are Bipolar (0x800 to 0x000 to 0x7FF), where the voltage 1/2 of V_{REF} is “0x000,” or Unipolar (0x000 to 0xFFF) is shown in the POLsel bit, bit 28. The POLsel bit of a Bipolar device is “1.” The analog value shown right after the MKY44-AD12A returns from reset depends on the sampling method. If the sampling method is single trigger mode, “0x000” will be shown until the first single trigger is received after returning from reset. During this time, “0x0” will be shown as the sequential number (SN) in bits 63 to 60. If the sampling method is not single trigger mode, the first A/D data will be shown after returning from reset.

(2) To refer to the status of the Di pins, read the 4-bit data of bits 15 to 12. The data of the general-purpose input pins (Di3 to Di0) depends on the setting of pin #DiInv. The setting status of pin #DiInv is shown in the DiInv bit, bit 30. If DiInv is “0,” the data will be shown by positive logic. In such a case, the status of the four general-purpose input pins will be shown as “0” when in Low-level and as “1” when in High-level. If the DiInv bit is “1,” the data will be shown by negative logic. Thus, the status of the general-purpose input pin will be shown as “1” when at Low-level and as “0” when at High-level.

(3) The setting condition and status of the MKY44-AD12A are shown in the 3 bits from bit 47 to 45 and 2 bits of bit 30 and bit 28. In bits 47 to 45, 30, and 28 (pins #DIP-DOSA7, #DIP-DOSA6, #MODsel, #DiInv, and #POLsel), the individual settings read out when returning from the reset are shown by positive logic.
TRGsel (trigger method selection), bit 31, shows the setting value stored inside of the MKY44-AD12A when returning from reset or the value set by the mail function.
PCsel (peak cut selection), bit 29, shows the setting value stored inside of the MKY44-AD12A when returning from reset or the value set by the mail function.

(4) The 4 bits from bit 63 to 60 show a sequential number (SN) that is increased by “0x1” for each update of the A/D conversion data. By referring to this sequential number, you can see that the data has been updated even when the analog number remains the same as before.
The sequential number goes up in the order of “0x1, 0x2.” After “0xF,” it goes back to “0x1.” If the sampling method is single trigger mode, “0x0” will be shown right after returning from the reset.

Stype1 (bit 47)	Stype0 (bit 46)	Sampling method
“0”	“0”	Cyclic
“0”	“1”	Single trigger
“1”	“0”	Period average
“1”	“1”	Moving average

	Description	“1”	“0”
MODsel (bit 45)	MODE selection	Setting mode	Operation mode
TRGsel (bit 31)	Trigger method selection	Software trigger	Hardware trigger
DiInv (bit 30)	Di logical inversion selection	Logical inversion	No logical inversion
PCsel (bit 29)	Peak cut selection	Cut the maximum and minimum values	Do not cut the maximum and minimum values
POLsel (bit 28)	Analog type selection	Bipolar: ±n V input	Unipolar: 0 V to + n V input

■ Output to the General-Purpose Output Pins

The MKY44-AD12A outputs to the general-purpose output pin the 4-bit (bits 3 to 0) data within the MB corresponding to the specified DOSA value.

Address	0x07	0x06	0x05	0x04	0x03	0x02	0x01	0x00
bit	63 to 4							3 to 0
	d.c.							Do

The part labeled “d.c.” (don’t care) in the table does not influence the operation of the MKY44-AD12A.

3	2	1	0
Do3	Do2	Do1	Do0

■ DIP-SW Settings for SA/DOSA

The MKY44-AD12A reads out the status of the 16 bits of pins #DIP-SA0 to #DIP-SA7 and #DIP-DOSA0 to #DIP-DOSA7 as the data for hardware setting when returning from a hardware reset. It is recommended to connect two 8-bit type DIP-SWs to these pins. These pins will be pulled up internally when reading out the DIP-SW and show "1" as the ON state (Low-level). The following shows MKY44-AD12A's definitions for the bits of the DIP-SWs for setting.

Pin	Name	DIP-SW No.		Signal		Function/Description
42	#DIP-DOSA7	DIP-SW/DOSA	8	Stype1		Select the sampling method for the analog value. Stype1, Stype0 = OFF, OFF Cyclic Stype1, Stype0 = OFF, ON Single trigger Stype1, Stype0 = ON, OFF Period average Stype1, Stype0 = ON, ON Moving average
41	#DIP-DOSA6		7	Stype0		
40	#DIP-DOSA5		6	DOSA	DOSA5	Set DOSA value in hexadecimal, treating the ON state as "1"
39	#DIP-DOSA4		5		DOSA4	
38	#DIP-DOSA3		4		DOSA3	
37	#DIP-DOSA2		3		DOSA2	
36	#DIP-DOSA1		2		DOSA1	
35	#DIP-DOSA0		1		DOSA0	

34	#DIP-SA7	DIP-SW/SA	8	BPS	BPS1	Set the transfer rate of CUnet. BPS1, BPS0 = OFF, OFF 12 Mbps BPS1, BPS0 = OFF, ON 6 Mbps BPS1, BPS0 = ON, OFF 3 Mbps BPS1, BPS0 = ON, ON (This setting is disabled.)
33	#DIP-SA6		7		BPS0	
32	#DIP-SA5		6	SA	SA5	Set DOSA value in hexadecimal, treating the ON state as "1"
31	#DIP-SA4		5		SA4	
30	#DIP-SA3		4		SA3	
29	#DIP-SA2		3		SA2	
28	#DIP-SA1		2		SA1	
27	#DIP-SA0		1		SA0	

■ Setting of Pins #MODsel, #POLsel, #DoClr, and #DiInv

The MKY44-AD12A has pins MODsel, #POLsel, #DoClr, and #DiInv to set various functions.
The MKY44-AD12A obtains the status of these setting pins when returning from a hardware reset. These pins will be pulled up internally when reading out the DIP-SW and show "1" as the ON state (Low-level). Activate the MKY44-AD12A after setting these pins to fit the user application.

MKY44-AD12A		Description	Function	
Pin	Name		Lo-input	Hi-input (open pin)
15	#Dilnv	Di logical inversion selection	Logical inversion	No logical inversion
16	#DoClr	Do pin clear selection when in DONA	Clear Do pin when in DONA	Do not clear Do pin when in DONA
17	#POLsel	Analog input type selection	Bipolar: ±n V input	Unipolar: 0 V to +n V input
18	#MODsel	Mode selection	Setting mode	Operation mode

Note: DONA means that the data can not be sent to MKY44-AD12A because the device (master) to write the data of CUnet shared memory to Do0 to Do3 is out of cycle or the device itself is out of CUnet cycle and not connected to the master.

■ Extended Use of the CUnet Mail Function

The MKY44-AD12A supports “product inquiry” and “reading and writing the parameter” requests from the other CUnet station using the CUnet mail function.

● Product Inquiry Using the Mail Function

Upon receiving a message in product inquiry format using “CUnet ?” character string, the MKY44-AD12A replies to the requester using the basic format of the MKY44-AD12A (see below). You can make a product inquiry from any node that is a CUnet IC in MEM mode.
The product inquiry format and the basic format of reply from MKY44-AD12A is shown below.

Product inquiry format: Mail sending from the requester to the MKY44-AD12A
Mail data size:1

The basic format of reply from MKY44-AD12A: Mail sending from the MKY44-AD12A to the requester
Mail data size:3 (Successful), 2 (Failed)

◆ Product Inquiry Format（Requester→MKY44-AD12A）

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Ascii	**C**	**U**	**n**	**e**	**t**	**[sp]**	**?**	**[¥r]**
Hex	0x43	0x55	0x6E	0x65	0x74	0x20	0x3F	0x0D

◆ Basic Response Format of the MKY44-AD12A（MKY44-AD12A→Requester）

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Ascii	**A**	**D**	**1**	**2**	**A**	**[sp]**	***VN**	***Vn**
Hex	0x41	0x44	0x31	0x32	0x41	0x20	✻	✻

Address	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Ascii	**M**	✻	✻	✻	✻	✻	✻	✻
⇒ Hex	✻	MC	SA	DOSA	ST1	ST2	0x00	0x00

Address	0x10	0x11	0x12	0x13	0x14	0x15	0x16	0x17
Hex ⇒	TP		FS	NS	TA		TD	TBM
	LSB	MSB			LSB	MSB		

◆ Description of the Basic Format

Symbol	Name	Description	Valid range
*VN *Vn	Version Number	Shows the version number of the MKY44-AD12A in two ASCII characters. The version numbers start from “01.” *VN represents the tens place and *Vn represents the ones place.	01 to 99 (in ASCII)
MS	Message Status	Shows the status of mail contents. “M”(0x4D): Master Code Successful notification to “CUnet ?” product inquiry. ”N”(0x4E): NAK (Negative AcKnowledgement) Error notification to “CUnet ?” product inquiry.	“M”,“N” (in ASCII)
MC	Message Code	Shows the message (error) code of the mail. 0x00：When MS（Message Status）is “M”. 0xE1：Error code when MS（Message Status）is “N”. The format is irregular. 0xE2：Error code when MS（Message Status）is “N.” The mail data size is irregular.	0x00,0xE1,0xE2

(Continue)

◆ Description of the Basic Format

(Continued)

Symbol	Name	Description	Valid range
SA	DIP-SW/SA	Shows the DIP-SW/SA data shown in the section "**DIP-SW Settings for SA/DOSA.**"	0x00 to 0xFF
DOSA	DIP-SW/ DOSA	Shows the DIP-SW/DOSA data shown in the section "**DP-SW Settings for SA/DOSA.**"	0x00 to 0xFF
ST1	Status1	Shows the one-byte status shown in "**Data placement of the occupied memory block**" (page 3 of this document), where the 4 bits from bit 47 to 44 are the upper nibble and the 4 bits from bit 31 to 28 are the lower nibble.	0x00 to 0xFF
ST2	Status2	Bit 0 shows "1" when the setting of #DoClr pin is Lo. Bit 1 to bit 7 are "0."	0x00 to 0x01
TP	Time of Period	The setting value of the sampling interval in the period average and moving average sampling method is shown as two hexadecimal bytes (in units of 100 µs). Only even numbers are valid.	0x0002 to 0x2710 (2 to 10000: even numbers) Initial value 0x000A
FS	Function Settings	Bit 1 is PCsel of bit 29 shown in "**Data placement of the occupied memory block.**" Bit 0 is TRGsel of bit 31 shown in "**Data placement of the occupied memory block.**"	0x00 to 0x03 Initial value 0x03
NS	Number of Sample	The setting value of the sampling frequency in the period average and moving average sampling methods is shown as one hexadecimal byte.	0x02 / 0x04 / 0x08/ 0x10 Initial value 0x08
TA	Trigger Address	If the sampling method is software trigger mode, the setting value of the trigger target address will be shown as two hexadecimal bytes. This address shows the address within the shared memory (Global Memory) of CUnet.	0x000 to 0x1FF Initial value 0x000
TD	Trigger Data	If the sampling method is software trigger mode, the setting value of the trigger key data will be shown as one hexadecimal byte.	0x00 to 0xFF Initial value 0xFF
TBM	Trigger Bit Mask	If the sampling method is hardware trigger mode, the setting value of the bit mask to select the general-purpose input pin of the trigger target will be shown as one hexadecimal byte. With this setting, only one bit (one pin) will be selected.	0x01 / 0x02 / 0x04 / 0x08 Initial value 0x01

When the MS (Message Status) of 0x08 byte is "M", it indicates the message is sent successfully.
At that time, MC (Message Code) of 0x09 byte indicates 0x00. The setting data starts from SA and the mail data size is 3.

When the MS (Message Status) of 0x08 byte is "N", it indicates the error.
At that time, MC (Message Code) of 0x09 byte indicates 0xE1 or 0xE2. The 0x00 data starts from SA and the mail size is 2.

● Reading and Writing the Parameter Setting Using the Mail Function

You can read and write the parameter settings stored inside MKY44-AD12A using the CUnet mail function.
You can read the setting parameter from any node that is CUnet IC in MEM mode. However, writing to set the parameter is accepted only from the node set to DOSA.
The parameter settings that can be changed are TP (Time of Period), FS (Function Settings) , NS (Number of Sample), TA (Trigger Address) , TD (Trigger Data), TBM (Trigger Bit Mask).
The parameter setting change format and the basic format of parameter setting for MKY44-AD12A are shown below.

Parameter setting change format: Mail sending from the requester to MKY44-AD12A
Mail data size: Indicates "3" when "W" (Write) is set to MS (Message Status.)
Mail data size: Indicates "2" when "R" (Read)" is set to MS (Message Status.)
The data from 0x10 to 0x17 is unnecessary when "R" (Read) is set to MS (Message Status.)

The setting reply format: Mail sending from MKY44-AD12A to the requester
Mail data size: Indicates "3" when the mail is sent successfully.
Indicates "2" when the mail sending is failed.

◆ Parameter setting change format of MKY44-AD12A (Requester to MKY44-AD12A)

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Ascii	**A**	**D**	**1**	**2**	**A**	**[sp]**	***VN**	***Vn**
Hex	0x41	0x44	0x31	0x32	0x41	0x20	*	*

Address	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Ascii	**MS**	*	*	*	*	*	*	*
Hex	*	MC	SA	DOSA	ST1	ST2	0x00	0x00

Address	0x10	0x11	0x12	0x13	0x14	0x15	0x16	0x17
Hex	TP		FS	NS	TA		TD	TBM
	LSB	MSB			LSB	MSB		

◆ Description of Parameter setting change format

Symbol	Name	Description	Valid range
*VN *Vn	Version Number	Shows the version number of the MKY44-AD12A in two ASCII characters. The version numbers start from "01." *VN represents the tens place and *Vn represents the ones place.	01 to 99 (in ASCII)
MS	Message Status	Shows the status of mail contents. "W" (0x57): Write Write the parameter setting data to the inside of MKY44-AD12A. "R" (0x52): Read Read the parameter setting data from the inside of MKY44-AD12A.	"W","R" (in ASCII)
MC	Message Code	Fixed to 0x00.	0x00
SA	DIP-SW/SA	Shows the DIP-SW/SA data in the section of "**DIP-SW Settings for SA/DOSA.**"	0x00 to 0xFF
DOSA	DIP-SW/ DOSA	Shows the DIP-SW/DOSA data in the section of "**DIP-SW Settings for SA/DOSA.**"	0x00 to 0xFF
ST1	Status1	Shows the status of one-byte status shown in "**Data Placement of the Occupied Memory Block**" (page 3 of this document), where the 4 bits from bit31 to bit28 are the upper nibble and the 4 bits from bit 31 to bit 28 are the lower nibble.	0x00 to 0xFF
ST2	Status2	Bit 0 shows "1" when the setting of pin #DoClr is Low. Bit 1 to 7 are "0."	0x00 to 0x01

(Continue)

◆ Description of Parameter setting change format

(Continued)

Symbol	Name	Description	Valid range
TP	Time of Period	The setting value of the sampling interval in the period average and moving average sampling methods is shown as two hexadecimal bytes (in units of 100 μs). Only even numbers are valid.	0x0002 to 0x2710 (2 to 10000: even numbers) Initial value 0x000A
FS	Function Settings	Bit 1 is PCsel of bit 29 shown in "**Data placement of the occupied memory block.**" Bit 0 is TRGsel of bit 31 shown in "**Data placement of the occupied memory block.**"	0x00 to 0x03 Initial value 0x03
NS	Number of Sample	The setting value of the sampling frequency in the period average and moving average sampling methods is shown as one hexadecimal byte.	0x02 / 0x04 / 0x08/ 0x10 Initial value 0x08
TA	Trigger Address	If the sampling method is software trigger mode, the setting value of the trigger target address will be shown as two hexadecimal bytes. This address shows the address within the shared memory (Global Memory) of CUnet.	0x000 to 0x1FF Initial value 0x000
TD	Trigger Data	If the sampling method is software trigger mode, the setting value of the trigger key data will be shown as one hexadecimal byte.	0x00 to 0xFF Initial value 0xFF
TBM	Trigger Bit Mask	If the sampling method is hardware trigger mode, the setting value of the bit mask to select the general-purpose input pin of the trigger target will be shown as one hexadecimal byte. With this setting, only one bit (one pin) will be selected.	0x01 / 0x02 / 0x04 / 0x08 Initial value 0x01

◆ Basic Response Format of the Parameter Setting for MKY44-AD12A (MKY44-AD12A → Requester)

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	
Ascii	**A**	**D**	**1**	**2**	**A**	**[sp]**	***VN**	***Vn**	⇒
Hex	0x41	0x44	0x31	0x32	0x41	0x20	*	*	

Address	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	
Ascii	**MS**	*	*	*	*	*	*	*	
⇒ Hex	*	MC	SA	DOSA	ST1	ST2	0x00	0x00	⇒

Address	0x10	0x11	0x12	0x13	0x14	0x15	0x16	0x17
⇒ Hex	TP		FS	NS	TA		TD	TBM
	LSB	MSB			LSB	MSB		

◆ Description of the Basic Format of the Parameter Setting for MKY44-AD12A

Symbol	Name	Description	Valid range
*VN *Vn	Version Number	Shows the version number of the MKY44-AD12A in two ASCII characters. The version numbers start from "01." *VN represents the tens place and *Vn represents the ones place.	01 to 99 (in ASCII)
MS	Message Status	Shows the status of mail contents. "A" (0x41): ACK (ACKnowledgement) Successful notification to the setting change request. "N" (0x4E): NAK (Negative AcKnowledgement) Error notification to the setting change request.	"A","N" (in ASCII)
MC	Message Code	Indicates the message (error) code of the mail. For details, refer to the table which describes "the byte 0x09 of the MC (Message Code)."	0x00 to 0x08,0xD0,0xE0 to 0xE2
SA	DIP-SW/SA	Shows the DIP-SW/SA data in the section of "**DIP-SW Settings for SA/DOSA.**"	0x00 to 0xFF

(Continue)

◆ **Description of Parameter setting change format**

(Continued)

Symbol	Name	Description	Valid range
DOSA	DIP-SW/ DOSA	Shows the DIP-SW/DOSA data in the section of "**DIP-SW Settings for SA/DOSA.**"	0x00 to 0xFF
ST1	Status1	Shows the one-byte status shown in "**Data placement of the occupied memory block**" (page 3 of this document), where the 4 bits from bit 47 to 44 are the upper nibble and the 4 bits from bit 31 to 28 are the lower nibble.	0x00 to 0xFF
ST2	Status2	Bit 0 shows "1" when the setting of pin #DoClr is Low. Bit 1 to 7 are "0."	0x00 to 0x01
TP	Time of Period	The setting value of the sampling interval in the period average and moving average sampling methods is shown as two hexadecimal bytes (in units of 100 μs). Only even numbers are valid.	0x0002 to 0x2710 (2 to 10000: even numbers) Initial value 0x000A
FS	Function Settings	Bit 1 is PCsel of bit 29 shown in "**Data placement of the occupied memory block.**" Bit 0 is TRGsel of bit 31 shown in "**Data placement of the occupied memory block.**"	0x00 to 0x03 Initial value 0x03
NS	Number of Sample	The setting value of the sampling frequency in the period average and moving average sampling methods is shown as one hexadecimal byte.	0x02 / 0x04 / 0x08/ 0x10 Initial value 0x08
TA	Trigger Address	If the sampling method is software trigger mode, the setting value of the trigger target address will be shown as two hexadecimal bytes. This address shows the address within the shared memory (Global Memory) of CUnet.	0x000 to 0x1FF Initial value 0x000
TD	Trigger Data	If the sampling method is software trigger mode, the setting value of the trigger key data will be shown as one hexadecimal byte.	0x00 to 0xFF Initial value 0xFF
TBM	Trigger Bit Mask	If the sampling method is hardware trigger mode, the setting value of the bit mask to select the general-purpose input pin of the trigger target will be shown as one hexadecimal byte. With this setting, only one bit (one pin) will be selected.	0x01 / 0x02 / 0x04 / 0x08 Initial value 0x01

When the parameter settings are successfully changed using the mail function, the MKY44-AD12A sends a message in which the byte 0x08 of the MS (Message Status) is "A." In that case, 0x00 code is stored in the byte 0x09 of the MC (Message Code), and the setting data is noticed to the address after SA. The size of mail data at this time will be 3.

When the parameter settings using the mail function are failed, the MKY44-AD12A sends a message in which the byte 0x08 of the MS (Message Status) is "N." In that case, the code of the error description is stored in the byte 0x09 of the MC (Message Code), and 0x00 is stored in the address after SA. The size of mail data at this time will be 2.

The list of the byte 0x09 of the MC (Message Code) at parameter setting change is shown below.

◆ Description of the Byte 0x09 of the MC (Message Code)

MC (Message Code)	Description
0x00	When MS (Message Status) is “A”, the message has been sent successfully.
0x01	Cannot accept the setting change since it is not setting mode.
0x02	Cannot accept Write command from a node which does not match DOSA.
0x03	The received byte 0x09 (MC: Message Code) is not “0x00.”
0x04	The specified TP (Time of Period) is out of the valid range.
0x05	The specified NS (Number of Sample) is out of the valid range.
0x06	The specified TA (Trigger Address) is out of the valid range.
0x07	The specified TBM (Trigger Bit Mask) is out of the valid range.
0x08	The specified FS (Function Settings) is out of the valid range.
0xD0	The combination of setting values regarding the sampling is irregular and cannot be accepted.
0xE0	The first 8 bytes are irregular.
0xE1	The format is irregular.
0xE2	The mail data size is irregular.

The mail format used in changing parameter settings is different from the basic format of the MKY44-AD12A (when it is sent successfully) by one letter. The difference is “W” in byte 0x08 instead of “M.” Therefore, it is recommended to set the parameter is set by the following operation procedure.

1. First, execute “product inquiry” by the requester in CUnet and copy the content sent from the MKY44-AD12A to the mail send buffer. Then, change “M” to “W” in byte 0x08.
2. Among TP, FS, NS, TA, TD, and TBM in the mail send buffer, rewrite the items to change.
3. Send a message to the MKY44-AD12A.
4. When the parameter settings are successfully changed using the mail function, the MKY44-AD12A sends a message in ACK format in which byte 0x08 of the basic format is “A.” The changed values are stored in TP, FS, NS, TA, TD, and TBM in the ACK format.

When the MKY44-AD12A changes the parameter setting successfully using the mail function, the parameter setting data is stored to the inside of the MKY44-AD12A. Thus, even if the power of a MKY44-AD12A in normal mode is turned off and on, or if hardware reset is executed, the MKY44-AD12A will start operation using the changed parameter values.

Also, if the MKY44-AD12A could not change the parameter setting successfully using the mail function, it will return a NAK code message in which byte 0x08 of the basic format is “N.” In this case, the reason for the NAK will be shown in byte 0x09.

Parameter setting change of MKY44-AD12A using the mail function is accepted only when in the setting mode where pin #MODsel is Low-level and when the message is sent from the node set to DOSA.
If the parameter setting change message is received when in normal mode where pin #MODsel is High-level, or if the message is sent from a node which is not set to DOSA, it will return the NAK code message and the parameter setting will not be changed. Also, if the message does not match with the format or the value to change is not in the valid range, the MKY44-AD12A will return NAK code message and will not change the parameter setting.

If a message in which byte 0x08 of the basic format is “R” is sent to the MKY44-AD12A, you can receive ACK format where byte 0x08 is “A.” This will enable reconfirmation of the changed parameter settings.

To close parameter setting change using the mail function to start operation, execute hardware reset of the MKY44-AD12A by resetting the power in the normal mode where the High-level is set to pin #MODsel.

■ Configuration Example of the CUnet Analog Input Terminal with the MKY44-AD12A

As shown in the configuration diagram of the CUnet analog input terminal with the MKY44-AD12A, the signal of the MKY44-AD12A network interface (pins CU_TXE, CU_TXD, CU_RXD) is connected to CUnet via the recommended transceiver or pulse transformer. If the voltage to input to the analog input pins of the MKY44-AD12A is treated as ±n V (Bipolar) (the voltage 1/2 of the reference voltage input is "0x000"), set the Low-level to pin #POLsel of the MKY44-AD12A. With this setting, A/D conversion data representing "-2048 to 0 to 2047 (0x800 to 0x000 to 0x7FF)" will be stored in the shared memory of CUnet. If the voltage to input to the analog input pins of MKY44-AD12A is "0 V to + n V (Unipolar)," set the High-level to pin #POLsel of the MKY44-AD12A. With this setting, A/D conversion data representing "0 to 4095 (0x000 to 0xFFF)" will be stored in the shared memory of CUnet.

If hardware trigger mode is selected as the sampling method, input to Di0 to Di3 a trigger signal whose Low-level and High-level are more than 200 μs.

If the data cannot be transmitted to the MKY44-AD12A, such as when the communication cable of the MKY44-AD12A mounted A/D slave is disconnected or when the device to write the shared memory data in Do0 to Do3 goes out of communication, the DONA (Data Out Not Available) pin of the MKY44-AD12A will transit to High-level. Using the #DoClr pin setting, you can select whether to clear (set as "0x00") or maintain the general-purpose output pins Do0 to Do3 when the DONA pin transits from Low-level to High-level.

■ Performance of the 12-bit A/D Converter in the MKY44-AD12A

The following describes the performance of 12-bit A/D converter in the MKY44-AD12A.

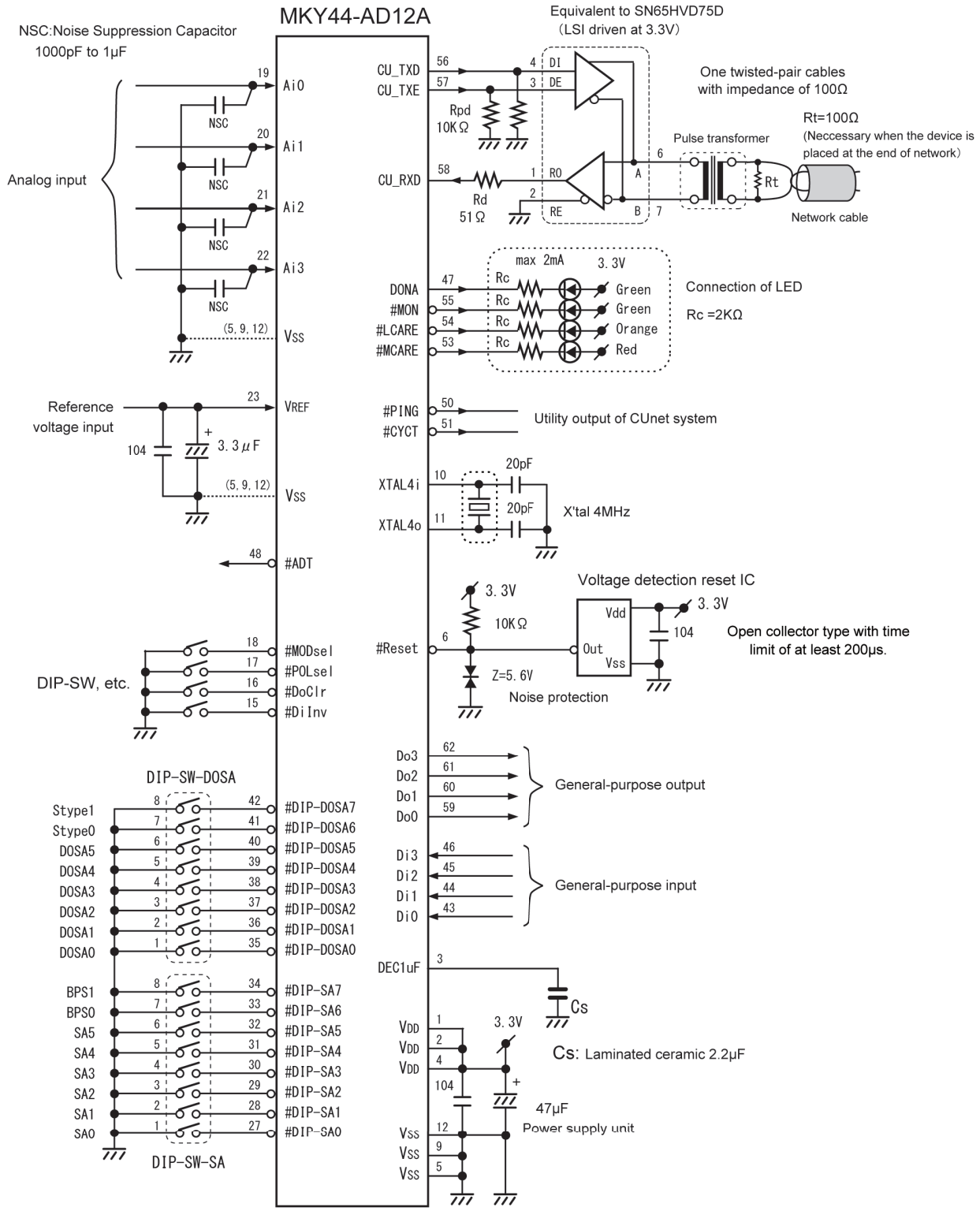
(Ta = -40 °C to +85 °C)

Description	Condition	Rating			Unit
		Minimum	Standard	Maximum	
Resolution	---	---	---	12	Bit
Non-linearity error	V_{DD} = 3.0 V V_{SS} = 0 V V_{REF} = 3.0 V	---	---	±3	LSB
Differential non-linearity error		---	---	±3	
Zero transition voltage		---	10	30	mV
Full-scale transition voltage		2970	2990	---	
A/D conversion time	---	---	26	---	μS
V_{REF} pin input voltage (reference voltage)	$V_{REF} \leq V_{DD}$	2.2	---	V_{DD}	V
Analog pin input voltage		V_{SS}	---	V_{REF}	
Leakage current of analog input pins	V_{Ai} = 0 V to V_{DD}	---	---	±1	μA

In order to stabilize the reference voltage in A/D conversion, connect a ceramic capacitor (0.1 μF) with a capacitor which has more than 3.3 μF near the MKY44-AD12A and between the V_{REF} and V_{SS} pins.
To the analog input (Ai0 to Ai3) pins, connect a signal source whose output impedance is less than 500 kΩ. Also, connect a capacitor of 1000 pF to 1 μF for noise suppression between the analog input pins and V_{SS} pin near the MKY44-AD12A.
The response time for changes in the analog input voltage involves the time constant provided by the output impedance of the signal source and the capacitor for noise suppression. For example, the time constant with 500 kΩ and 1 μF is 500,000 × 0.000001 = 0.5 seconds. In view of this time constant, select the constant that fits your application. In configuring the CUnet analog input terminal device using the MKY44-AD12A, you should prepare circuits that fit your application based on the consideration of these time constants, even when it requires an input buffer or filter circuit to input analog signals to the MKY44-AD12A.

Even if the voltage of the analog input (Ai0 to Ai3) pins exceeds V_{REF}, or if it falls below V_{SS}, the value will not become cyclic (e.g. 0x000 or 0x001 before 0xFFF) as the result of overflow. However, the value will not be guaranteed correct as an A/D conversion value. The voltage to apply to the analog input pins must be within the rated range.
Devices such as transceivers that drive CUnet communication cables will experience a large energy variation in signal transition. Similarly, if you need to control heavy load using general-purpose output pins, or if the drive performance of the signal source connected to general-purpose input pins is excessive, there will be a large energy variation in signal transition. To prevent the signal for A/D conversion from receiving adverse electrical effects from these, pay careful attention to the power supply ability of each power supplies, the arrangement of components on the board, and the wiring of signal cables. In particular, make sure that the signals involving CU_TXD, CU_TXE, and CU_RXD do not become parallel with or overlap the analog signals.

■ Configuration Diagram of the Analog Input Terminal



■ Signal in A/D Conversion

The MKY44-AD12A outputs the Low-level to pin #ADT (A/D Timing) in A/D conversion. By monitoring this pin, you can confirm the execution of A/D conversion.

■ Pin Functions of the MKY44-AD12A

Pin name	Pin No.	Logic	I/O	Function
DEC1UF	3	--	--	Connect a capacitor whose effective capacitance is at least 1 μF and a 0.1 μF ceramic capacitor for high frequency bypass in parallel between this pin and Vss. Or connect a laminated ceramic capacitor of around 2.2 μF with the property that capacitance reduction is about 20% even in DC bias.
#Reset	6	Negative	I	The hardware reset input pin of MKY44-AD12A. Right after power is turned on or when the user intentionally resets the hardware, Low should be retained for at least 200 μs.
XTAL4i XTAL4o	10, 11	--	--	Pins to connect a crystal resonator. Connect a 4 MHz crystal resonator between these pins. Connect 20 pF ceramic capacitors between these pins and Vss. The layouts must be respectively near the pins. When connecting oscillator, input the clock signal to XTAL4i as shown below and leave XTAL4o to be opened. Clock frequency : 4 MHz ±500 ppm Jitter : Within 500 ps Rise / Fall time : Within 20 ns (VDD 20% - 80% threshold)
#DiInv	15	Negative	I	Pin to set logical inversion of Di0 to Di3.
#DoClr	16	Negative	I	Setting pin to clear pins Do0 to Do3 when in DONA.
#POLsel	17	Negative	I	Pin to set whether the analog input value should be treated as Bipolar (±n V) or Unipolar (0 V to+n V).
#MODsel	18	Negative	I	Pin to set the mode of the MKY44-AD12A.
Ai0	19	Positive	AI	Ch0 analog signal input pin.
Ai1	20	Positive	AI	Ch1 analog signal input pin.
Ai2	21	Positive	AI	Ch2 analog signal input pin.
Ai3	22	Positive	AI	Ch3 analog signal input pin.
Vref	23	Positive	AI	Pin to input the reference voltage of the 12-bit A/D converter.
#DIP-SA7 to #DIP-SA0	27 to 34	Negative	I	Pins to connect a DIP-SW or such to set the SA and BPS values. Set the SA value in hexadecimal, treating the ON state as “1.”
#DIP-DOSA7 to #DIP-DOSA0	35 to 42	Negative	I	Pins to connect a DIP-SW or such to set the DOSA and Stype values. Set the DOSA value in hexadecimal, treating the ON state as “1.”
Di0 to Di3	43 to 46	Positive	I	4 bits of general-purpose input pins. Leave these pins open when not in use (internal pull-up).
DONA	47	Positive	O	This pin retains the High-level during the DONA (DO Not Arrival) state. It is at Low-level at other times.
#ADT	48	Negative	O	Monitor pin for A/D conversion operation. This pin outputs the Low-level during A/D conversion.
#PING	50	Negative	O	A pin to output the PING signal, which is a standard function of CUnet. When the PING signal occurs, this pin transitions to Low-level.
#CYCT	51	Negative	O	A pin to output the CYCT signal, which is a standard function of CUnet. When the CYCT signal occurs, this pin transitions to Low-level.
#MCARE	53	Negative	O	A pin to output the MCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for about 50 ms, when the MCARE signal occurs and when it returns from hardware reset. It is recommended to connect red color LED indicating a definite warning to this pin.
#LCARE	54	Negative	O	A pin to output the LCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for about 50 ms, when the LCARE signal occurs and when it returns from hardware reset. It is recommended to connect orange color LED indicating a gentle warning to this pin.
#MON	55	Negative	O	A pin to output the MON signal, which is a standard function of CUnet. This pin retains Low-level while a link has been established with another CUnet station for at least 3 consecutive cycles. It is recommended to connect green color LED indicating a stable operation to this pin.
CU_TXD	56	Positive	O	An output pin to send CUnet packets. Connect this pin to a drive input pin such as of a driver.
CU_TXE	57	Positive	O	A pin to output the High-level while CUnet packets are output. Connect this pin to the enable input pin of the driver.
CU_RXD	58	Positive	I	A pin to input CUnet packets. Connect this pin to the output pin of the receiver.
Do0 to Do3	59 to 62	Positive	O	4-bit general-purpose output pin. Leave this pin open when not in use.
VDD	1, 2, 4			Power pin. Supply 3.3 V.
Vss	5, 9, 12			Power pin. Connected to 0 V.
N.C.	7, 8, 13, 14, 24, 25, 26, 49, 52, 63, 64			Do not connect to other signals; keep them open.

■ Monitor pins of CUnet

Pin	Function
#PING	This pin normally maintains High-level. It transitions to Low-level when the PING instruction is received from another CUnet station, and later it transitions to High-level when a packet with no PING instruction to MKY44-AD12A is not placed is received from another CUnet station.
#CYCT	This pin normally maintains High-level and outputs Low pulse for "2 × Tbps" time at the lead timing of the CUnet cycle. Tbps is 83.33 ns at 12 Mbps, 166.67 ns at 6 Mbps, and 333.33 ns at 3 Mbps.
#MON	This pin outputs the MON signal, which is a standard function of CUnet. This pin retains Low-level while a link has been established with another CUnet station for at least 3 consecutive cycles.
#LCARE	This pin outputs the LCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for 50 ms when the LCARE signal is generated and upon return from hardware reset. Also, this pin outputs the Low-level to display hardware errors, including setting errors.
#MCARE	This pin outputs the MCARE signal, which is a standard function of CUnet. This pin outputs the Low-level for 50 ms when the MCARE signal is generated and upon return from hardware reset. Also, this pin outputs the Low-level to display hardware errors, including setting errors.
DONA	This pin outputs the Low-level when the master set in DOSA is connected. When it has not confirmed the presence of another party in the past 16 consecutive cycles, it outputs the High-level.

■ Connection of LEDs and Display Status

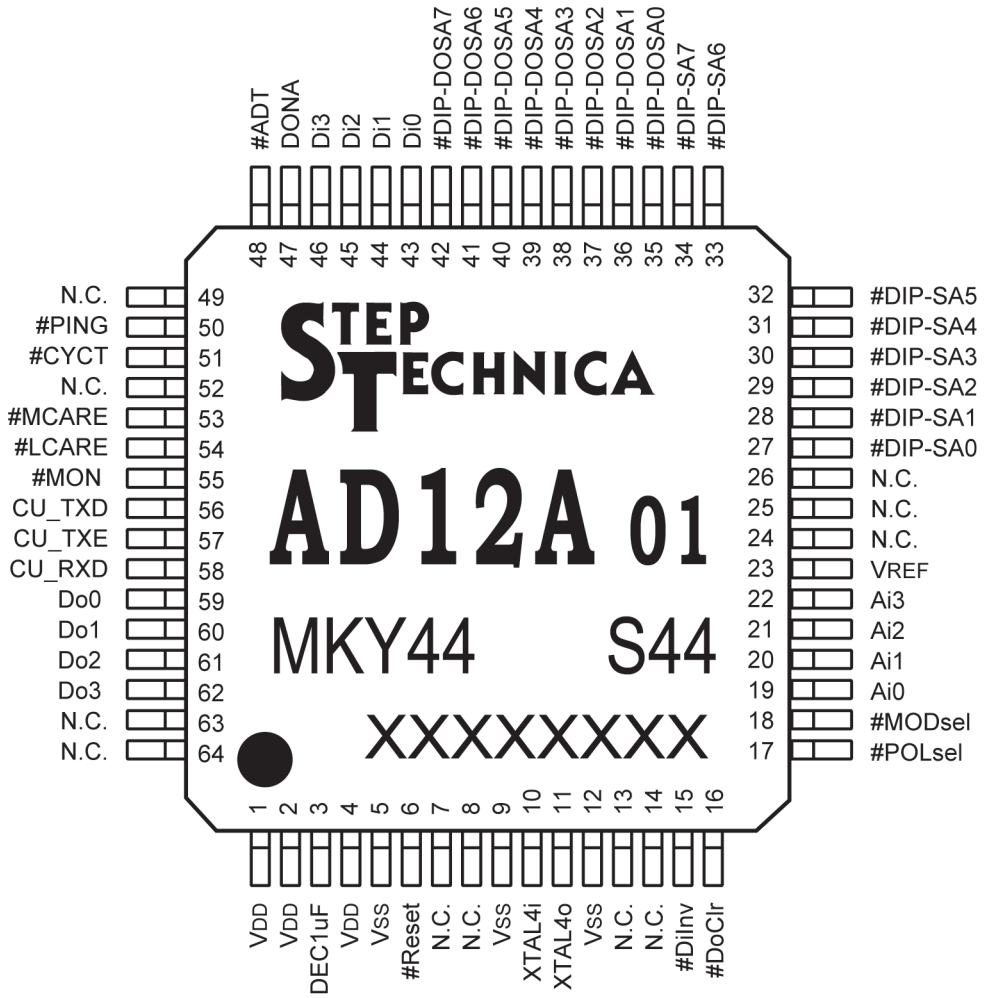
LED connection is recommended for the #MON, #LCARE, #MCARE, DONA pins of MKY44-AD12A. It is recommended to connect green color LED part indicating a stable operation to #MON pin and DONA pin. To #LCARE pin, it is recommended to connect orange color LED part indicating a gentle warning. To #MCARE pin, it is recommended to connect red color LED part indicating a definite warning. These pins have ±2mA current drive capability. Connect them in such a way that the LEDs will light up at Low-level.
The LEDs display the status of MKY44-AD12A. The state in which MON and DONA are lit is when normal operation is possible.
Note: The following table does not cover the pin name "#" that shows negative logic, since it is based on signal names.

DONA	MON	LCARE	MCARE	State
---	---	---	---	Indicates the state of power off, the state when the #Reset pin is active, or the state when no CUnet station is linked after returning from hardware reset.
---	●	---	---	Although a link is successfully established with at least one CUnet station, the station address device (the other party that writes the data to the MKY44-AD12A) set by DOSA is missing.
●	●	---	---	The connection of the CUnet network is normal.
---	---	---	●	The setting values of SA and DOSA of DIP-SW are inappropriate.
●	---	---	---	Indicates that the packet sent from the station set to DOSA can be received in OC (Out of Cycle) state.
---	---	□	---	When it becomes clear that at least one CUnet link is not established, the LED will be lit for approximately 50 ms.
---	---	---	□	When it becomes clear that at least one CUnet link has not been established during the last 3 consecutive scans, the LED will be lit for approximately 50 ms.
---	---	□	□	When it becomes clear that at least one CUnet link has been disconnected during the last 3 consecutive scans, and when hardware reset is executed, the LED will be lit for approximately 50 ms.
---	---	▲	▲	The following internal hardware of MKY44-AD12A is abnormal. Blink alternately every second ⇒ DIP-SW read hardware Blink alternately every two seconds ⇒ MKY44-AD12A internal hardware Please perform maintenance such as replacement.

●: Continuous lighting □: Lit for about 50 ms ▲: Alternating lit and unlit every few seconds

Unique to MKY44-AD12A display, the status in which only MCARE stays lit means that the settings of SA and DOSA of DIP-SW are inappropriately identical or overlapping values. If LCARE and MCARE keep blinking every few seconds, it means a failure caused by a crash in MKY44-AD12A.
The other signal transitions of MON, LCARE, and MCARE are standard CUnet operation. For more information about these signals, refer to ***"4.4.5 Network Quality Management and Display"*** in the User's Manual of the master MKY43.

■ Pin Assignment



Note: N. C. pin is not connected. Pins prefixed with "#" are negative logic (active Low).

■ Electrical Ratings

(T_A = 25°C V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	---	-55	---	125	°C
Operating temperature	Topr	---	-40	---	85	°C
Pin voltage (absolute maximum rating)	V_I	---	-0.3	---	V_{DD}+0.3	V
Operating power supply voltage	V_{DD}	---	3.0	3.3	3.6	V
Mean operating current	$V_{DD}A$	Vi = V_{DD} or V_{SS}, output open XTAL = 4 MHz	---	10	20	mA
I/O pin capacitance	Ci/o	V_{DD} = Vi = 0 V Ta = 25°C	---	10	---	pF
Rise/fall time of input signal	T_{ICLK}	When inputting generated clock of XTAL4i pin	---	---	5	ns
Rise/fall time of input signal	T_{IRF}	Schmitt trigger input	---	---	100	ms

■ Pin Ratings

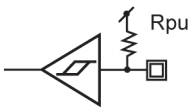
No	I/O	Name	Type
1	--	V_{DD}	--
2	--	V_{DD}	--
3	--	DEC1uF	--
4	--	V_{DD}	--
5	--	V_{SS}	--
6	I/O	#Reset	C
7	--	N.C.	--
8	--	N.C.	--
9	--	V_{SS}	--
10	--	XTAL4i	--
11	--	XTAL4o	--
12	--	V_{SS}	--
13	--	N.C.	--
14	--	N.C.	--
15	I	#DiInv	A
16	I	#DoClr	A

No	I/O	Name	Type
17	I	#POLsel	A
18	I	#MODsel	A
19	AI	Ai0	D
20	AI	Ai1	D
21	AI	Ai2	D
22	AI	Ai3	D
23	AI	V_{REF}	E
24	--	N.C.	--
25	--	N.C.	--
26	--	N.C.	--
27	I	#DIP-SA0	A
28	I	#DIP-SA1	A
29	I	#DIP-SA2	A
30	I	#DIP-SA3	A
31	I	#DIP-SA4	A
32	I	#DIP-SA5	A

No	I/O	Name	Type
33	I	#DIP-SA6	A
34	I	#DIP-SA7	A
35	I	#DIP-DOSA0	A
36	I	#DIP-DOSA1	A
37	I	#DIP-DOSA2	A
38	I	#DIP-DOSA3	A
39	I	#DIP-DOSA4	A
40	I	#DIP-DOSA5	A
41	I	#DIP-DOSA6	A
42	I	#DIP-DOSA7	A
43	I	Di0	A
44	I	Di1	A
45	I	Di2	A
46	I	Di3	A
47	O	DONA	B
48	O	#ADT	B

No	I/O	Name	Type
49	--	N.C.	--
50	O	#PING	B
51	O	#CYCT	B
52	--	N.C.	--
53	O	#MCARE	B
54	O	#LCARE	B
55	O	#MON	B
56	O	CU_TXD	B
57	O	CU_TXE	B
58	I	CU_RXD	A
59	O	Do0	B
60	O	Do1	B
61	O	Do2	B
62	O	Do3	B
63	--	N.C.	--
64	--	N.C.	--

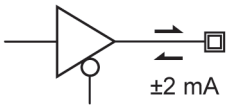
Type-A Pull-up resistor Schmitt input



V_{t+} max = 0.8 × V_{DD}
V_{t-} min = 0.2 × V_{DD}
ΔV_t min = 0.6 V

Rpu (Pull-up resistor) Typ:100 KΩ (30 KΩ to 300 KΩ:V_{DD} = 3.0 V, V_I = V_{SS})

Type-B Push-pull output



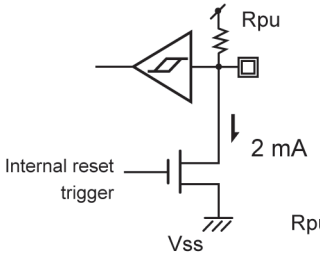
Internal reset signal

V_{OH} min = 2.4 V (V_{DD} = 3.0 V, I_{OH} = -2 mA)
V_{OL} max = 0.4 V (V_{DD} = 3.0 V, I_{OL} = 2 mA)

I_{OH} max = -2 mA
I_{OL} max = 2 mA

The Type-B output pin is in a high impedance state during hardware reset.
For user application devices for which this state is inappropriate, connect to the pin either pull-down resistance or pull-up resistance that can ensure initial levels suitable for the user appreciation.

Type-C Pull-up resistor Schmitt input Open drain output

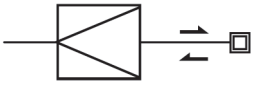


V_{t+} max = 0.8 × V_{DD}
V_{t-} min = 0.2 × V_{DD}
ΔV_t min = 0.6 V

V_{OL} max = 0.4 V (V_{DD} = 3.0 V, I_{OL} = 2 mA)
I_{OL} max = 2 mA

Rpu (Pull-up resistor) Typ:100 KΩ (30 KΩ to 300 KΩ:V_{DD} = 3.3 V, V_I = V_{SS})

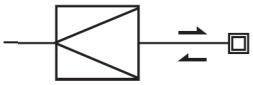
Type-D Analog input



V_{Ai} max = V_{REF}
V_{Ai} min = V_{SS}

I_{Ai} max = ±1 μA (Leak)

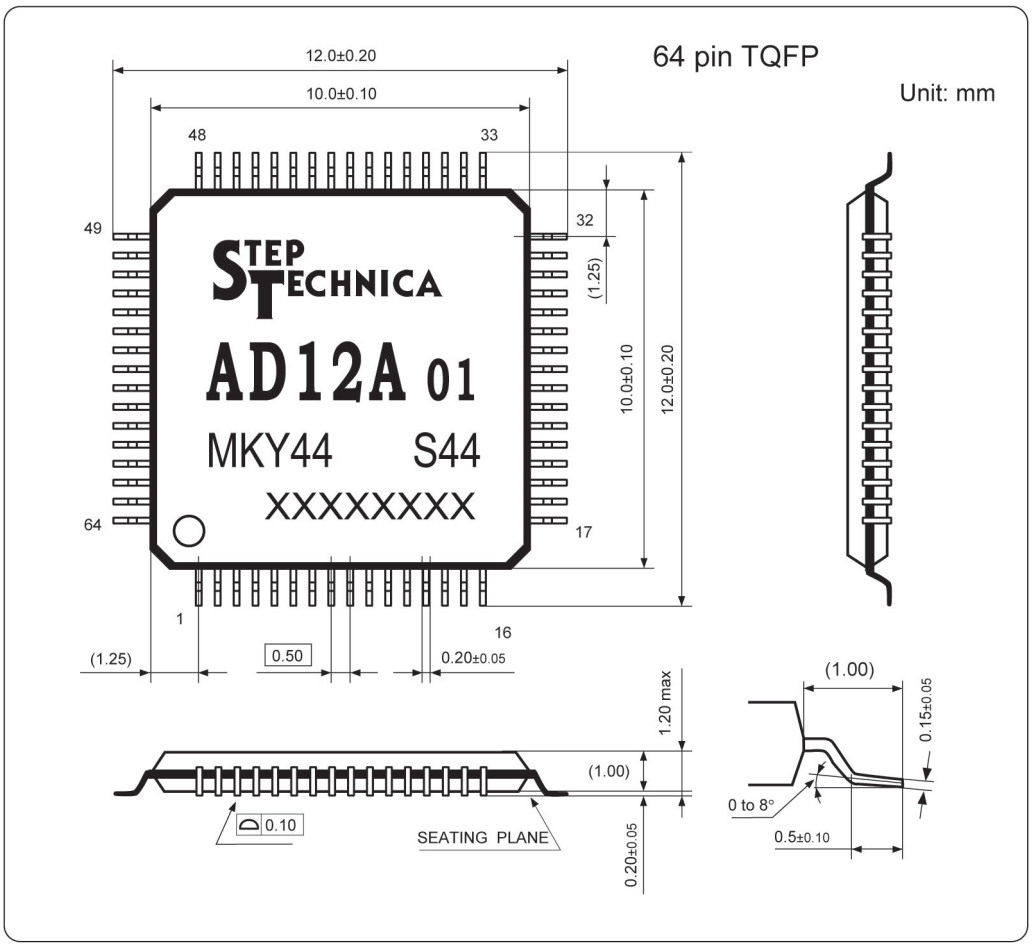
Type-E Reference voltage input



V_{Ai} max = V_{DD}
V_{Ai} min = 2.2 V

I_{Ai} max = ±1 μA (Leak)

■ Package Dimensions



Revision History

Version	Data	Page	Contents
1.1E	NOV 2013		Issued the first edition
1.2E	OCT 2020	P9	Added the functional description for XTAL4i and XTAL4o
1.3E	APR 2021	P5	Revised the format description in "Product Inquiry Using the Mail Function" and "Parameter Setting Change Using the Mail Function" of "Extended use of the CUnet mail function."
		P14	Added the description in lighting state of DONA.
		-	Corrected typos and errors in the whole document.
1.4E	JAN 2024	P18	Change of address

Document No.: DS_MKY44AD12A_V1.4E
Issued: January, 2024

Related Manuals:

CUnet Introduction Guide		**STD_CUSTU_Vx.xE**
CUnet Technical Guide		**STD_CUTGN_Vx.xE**
CUnet IC	**MKY43 User's Manual**	**STD_CU43_Vx.xE**
CUnet I/O- IC	**MKY46 User's Manual**	**STD_CU46_Vx.xE**
CUnet HUB- IC	**MKY02 User's Manual**	**STD_CUH02_Vx.xE**

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